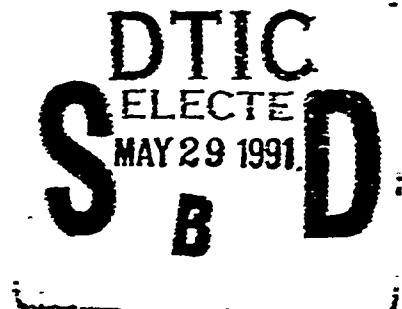e900901

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13th Annual Electronics Manufacturing Seminar Proceedings

Sponsored by
Electronics Manufacturing Productivity Facility
and
Soldering Technology Branch

1-3 March 1989

**NAVAL WEAPONS CENTER
CHINA LAKE, CA 93555-6001**

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Naval Weapons Center

FOREWORD

The proceedings contained herein are compiled and published by the Engineering Department, Naval Weapons Center, as supporting documentation for the 13th Annual Electronics Manufacturing Seminar to be held on 1-3 March 1989 at NWC, China Lake, Calif. This document is a compilation of information that was provided by both nongovernment and governmental sources.

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January 1989

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Copies of specific articles should be requested from the individual authors.

NWC Technical Publication 6986
EMPF Technical Report 0007

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED			1b. RESTRICTIVE MARKINGS			
2a. SECURITY CLASSIFICATION AUTHORITY			3. DISTRIBUTION/AVAILABILITY OF REPORT A Statement; approved for public release; distribution is unlimited			
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE						
4. PERFORMING ORGANIZATION REPORT NUMBER(S) NWC TP 6986			5. MONITORING ORGANIZATION REPORT NUMBER(S)			
6a. NAME OF PERFORMING ORGANIZATION Naval Weapons Center	6b. OFFICE SYMBOL (if applicable)		7a. NAME OF MONITORING ORGANIZATION			
6c. ADDRESS (City, State, and ZIP Code) China Lake, CA 93555-6001			7b. ADDRESS (City, State, and ZIP Code)			
8a. NAME OF FUNDING/SPONSORING ORGANIZATION	8b. OFFICE SYMBOL (if applicable)		9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER			
8c. ADDRESS (City, State, and ZIP Code)			10. SOURCE OF FUNDING NUMBERS			
			PROGRAM ELEMENT NO	PROJECT NO	TASK NO	WORK UNIT NO

11. TITLE (include Security Classification)

Proceedings of the Thirteenth Annual Electronics Manufacturing Seminar (U)

12. PERSONAL AUTHOR(S)

13a. TYPE OF REPORT Annual	13b. TIME COVERED FROM 88 Mar TO 89 Feb	14. DATE OF REPORT (Year, Month, Day) 1989, March	15. PAGE COUNT 420

16. SUPPLEMENTARY NOTATION

17.	COSATI CODES		18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)	
FIELD	GROUP	SUB-GROUP	Automated inspection	Circuit boards
09	01		Automated solder application	Cleanability
13	05/08		CCAPS	Cleaning alternatives (See back of form)

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

(U)   Presented are the proceedings of the 13th Annual Electronics Manufacturing Seminar, held on 1–3 March 1989 at the Naval Weapons Center, China Lake, Calif. The proceedings include the papers presented at the Seminar and cover all aspects of soldering technology and electronics manufacturing. The proceedings are a compilation of information provided by both nongovernment and government sources. The proceedings are published in the interest of furthering communication and broadening awareness of current activities among soldering technology and electronics manufacturing specialists.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT ☐ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION Unclassified	
22a. NAME OF RESPONSIBLE INDIVIDUAL John W. Boutwell	22b. TELEPHONE (Include Area Code) (619) 939-1800	22c. OFFICE SYMBOL Code 3681

DD FORM 1473, 84 MAR   83 APR edition may be used until exhausted   SECURITY CLASSIFICATION OF THIS PAGE
                              All other editions are obsolete

18. (Cont.)

Conformal coating repair
Design duty cycle
Durability test development
Electronic system verification
Environmental stress screening
Fatigue life/strain range
Hazardous Materials (HAZMAT) Program
Infrared inspection
Laminography
Laser soldering
Leadless devices
Manufacturing screening
Montreal Protocol
Multilayer boards
Power supply reliability
Preformed elastomeric sheet adhesive
Printed wiring assembly
Public land resources
Residue prevention
Robotic soldering system
Solderability
Solder joint inspection
Solder preforms
Stratospheric ozone
Surface-mount technology
Test, analyze, and fix (TAAF) procedures
Test methods
Thermal fatigue
Thermal stress
Wave soldering
Wetting balance

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INTRODUCTION

The ever-changing, fast-paced technological advances being made today in electronics manufacturing present a challenge to us all. To help meet this challenge, we must work together. This Seminar—the 13th Annual Electronics Manufacturing Seminar—gives us an excellent opportunity to do just that. This Seminar promotes an open exchange of information on all issues of electronics manufacturing. It provides a forum for all persons involved in this technology, whether from government, industry, or academia. Here we can openly discuss these issues and share our ideas. Here we can work together toward our common goal: to improve the U.S. electronics industrial base.

To help make this improvement we must continue to work toward the goals of productivity, producibility, and quality. We must maintain a concerted effort to resolve production-line problems. Then, we must develop process controls and methods to solve them. Because productivity, producibility, and quality are inseparable, it is critical that our designers learn from past problems and that they design for ease of manufacturing. The Navy is continuing to work with industry through the efforts of the Electronics Manufacturing Productivity Facility (EMPF) and the Naval Weapons Center Soldering Technology Branch.

The Soldering Technology Branch is continually working to ensure that we meet the goals of producibility and quality. We evaluate soldering requirements and provide these evaluations to government and industry facilities. The Navy's work to consolidate its soldering requirements has resulted in WS-6536E, and we are continuing to work with DOD-STD-2000.

Another approach to improve our electronics industrial base is coordinated by the Naval Industrial Resources Support Activity (NAVIRSA) Detachment EMPF. The EMPF is leading the cooperative effort between electronic equipment manufacturers, product manufacturers, and government agencies to research, develop, and demonstrate electronics manufacturing processes and materials. The EMPF coordinates the cooperative work of these groups to develop high-quality processes and to demonstrate manufacturing disciplines in a production environment. The EMPF documents this cooperative work and develops an accessible information source for electronics manufacturing productivity. Our goal is to gain information, share information, and use information to help produce high-quality products at lower cost in less time.

We are indeed looking forward to working with you to improve our electronics industrial base.

We appreciate your interest in electronics manufacturing and thank you for joining us at this Seminar.

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ASSESSING SOLDERABILITY PERFORMANCE
WITH WETTING BALANCE INDICES AND DISCRIMINANT ANALYSIS

by

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ABSTRACT

Currently, visual inspection provides the means for assessing
component lead solderability in much of the integrated circuit
industry. Methods of quantifying solderability performance based on
wetting balance data have been proposed by numerous authors. Section I
of this paper provides background and describes several solderability
indices and criteria including John Devore's coefficient of wetting and
solderability index, James Woolridge's criteria, industry criteria and
stability of wetting index described by Gert Becker and the MIL-STD
883C TM2022 solderability test.

At central issue is identifying wetting balance parameters which
may be used to construct solderability indices of predictive value for
solderability performance. This paper addresses four main topics: (1)
Section II introduces and describes new solderability indices which may
be of value in determining solderability results; (2) Section III,
gives the experimental technique used and explores correlations among
the solderability indices and criteria described in Sections I and II;
(3) Section IV uses discriminant analysis to identify wetting balance
parameters which exhibit predictive value in assessing solderability
performance and deve.ops discriminant functions that predict
solderability more accurately than any of the individual parameters
identified above. (4) In Section V, the identified wetting balance
parameters determined in Section IV are used in an actual manufacturing
process field example to predict solder coverage on the leads of
ceramic dual in-line packages. Correlation between 10X visual
inspection and the predicted values of solder coverage is reported.

SECTION I. INTRODUCTION

In the manufacture of electronic equipment most components are
interconnected by some form of mass soldering technique in which a

large number of joints are soldered simultaneously. Regardless of how the soldering is accomplished, e.g. wave solder, I.R. or vapor phase reflow, the conditions must be favorable so that the molten solder immediately wets to the components and board circuit pattern. This ability of a surface to metallurgically accept molten solder during the soldering operation is known as the solderability of the surface.

DeVore (reference 1) cites three recognized mechanisms of solderability: wetting, non-wetting and dewetting. Full metallurgical wetting producing fast and complete intermetallic formation is the desired condition for soldering. This requires a clean interface which must remain clean during the intermetallic formation; otherwise one of the undesirable conditions of dewetting or non-wetting will occur. Nonwetting, the opposite extreme of wetting, results from the presence of a physical barrier between the base metal and the solder. The underlying action of dewetting has been the least understood of the solderability mechanisms. Visually, dewetting is characterized by solder on the surface pulling back into irregular mounds. A more in-depth explanation of soldering mechanisms with reference to detecting these mechanisms using a wetting balance is given by DeVore (reference 1).

In order to avoid difficulties caused by non-wetting and dewetting, it has been necessary to test the solderability of components and boards before assembly. The two popular methods of solderability testing are the use of extended steam aging followed by either visual inspection or wetting balance testing.

Currently, visual or optical criteria are the primary methods of assessing solderability throughout the industry. It is very easy to determine full wetting and most non-wetting conditions using these criteria. However, visual inspection is inherently subjective and operator dependent.

By contrast, the wetting balance can give an objective assessment of the solderability of the surface. The value of an objective method over the dip-and-look test for solderability has been recognized by other authors, (references 2 and 3). Occasions exist where non-wetting on some base metals are difficult to detect visually. For example, visual difficulties may be experienced when nickel and nickel-iron alloys, both close in color to solder, are employed (reference 1). Use of the wetting balance avoids these problems.

However, in order to successfully use wetting balance curves to assess solderability, the information from the curve must be related to the corresponding solderability mechanism. For instance, dewetting, which is the most complex of the solderability mechanisms, can only be seen visually as solder pullback. The lesser degrees of dewetting are difficult to detect visually, but may be revealed on the wetting

balance by shakes on the curve and by an extreme withdrawal force
(references 1 and 2). Non-wetting is graphically displayed on the
wetting balance by markedly low wetting forces (perhaps not even
achieving positive values).

In recent years there have been numerous attempts to correlate
wetting balance criteria to visual criteria (references 1-6). Problems
that exist with this type of correlation are complicated by differences
in heat demand of various specimens (reference 4 and 5) and differences
in characteristic curves produced by the wetting balance for the
particular surface geometry under test. For example, a solid metal
lead, a PWB and an LCC will typically exhibit distinctive wetting
balance curves (reference 6). However, once corrections are made for
surface geometry and buoyancy, the general shape of the curves tend to
appear more similar.

It is the intent of this paper to summarize the wetting balance
parameters studied in references 1-6 for both through hole and surface
mount applications and extend them to multi-leaded I.C. packages. This
study considers wetting balance curve relationships to visual criteria
for ceramic dual in-line packages (CERDIPs). Additionally, new indices
are proposed and both new and current indices are examined
statistically to determine correlation with visual criteria. The
ultimate objective is to find ways to utilize the wetting balance in a
real time production environment to predict solderability on the basis
of a few test units. Some of the difficulties in achieving this goal
have been documented by Woolridge (reference 6).

Figure 1 displays a typical wetting balance curve along with
notation for curve measurements used in this paper. Note that $t_{(i)}$
denotes a time taken at the ith second while t_a denotes a time
taken at a particular event. For example, $t_{(1)}$, $t_{(2)}$, $t_{(2.5)}$
$t_{(4.5)}$ and $t_{(5)}$ refer to times taken after the respective intervals
1, 2, 2.5, 4.5, and 5 seconds. The values t_0, t_{end}, t_{eq}, t_{max},
t_{min}, t_{spike}, and t_{tan} refer to times taken at the point the
curve recrosses the time axis, the end of the test at which the unit is
started to be removed from the solder pot, the equilibrium point at
which the curve maintains a constant value to the end of the test, the
point at which the curve first reaches a maximum, the point at which
the curve first reaches a minimimum, the spike point on the withdrawal
and the curve tangent (defined in the next section), respectively.
Similar definitions hold for the quantities F_i on the force axis in
Figure 1. Note that all force measurements used are corrected for
buoyancy and perimeter by the transformation,

$$F_i = (F_{i,uncorrected} + F_b)/p \qquad (1)$$

where p is the cross sectional perimeter coplanar with the solder

surface for the object being immersed and $F_b = \rho$ g V is the correction due to the buoyancy force comprised of ρ = density of molten solder (8.15 g/cm^3 for Sn63 solder), g = acceleration due to gravity (980 cm/sec^2) and V = volume of the object immersed in solder. All references to events are to a particular graph not to a set of graphs, i.e. the event of reaching a maximum, for instance, is determined from a particular graph and is not intended to be a property of an entire group of units.

With this notation, Table 1 presents descriptions and acronyms for the current solderability tests and indices studied in this paper. The indices and tests presented in Table 1 may be grouped according to the concerns each is designed to detect. Notice that all have elements of speed and force except for the stability of wetting, (SW) which is designed to access dewetting exclusively. Only DeVore's Solderability Index (SI) contains components to check for all three attributes, speed, force and dewetting.

SECTION 2. PROPOSED INDICES

At the core of providing an index to access solderability are the attributes of speed and strength of wetting. In this section, five new wetting balance indices are defined.

The first new index is concerned with using the maximum wetting force, F_{max}, to access solderability. We shall define:

$$MAXANG = \tan^{-1}(F_{max}/t_{max}) \tag{2}$$

as the angle formed between the time axis and the line connecting the point of maximum wetting force, M, with the origin (start of test). This is shown in Figure 2. Although MAXANG is similar to the coefficient of wetting index (CW), it is able to be computed in more cases than CW. An equilibrium point is necessary for CW to be defined and waiting for equilibrium to be reached may require an excessively long test time. One other difficulty with equilibrium experienced in actual experimentation is the problem of identification. Some subjectivity is introduced in trying to decide just when the graph is truly constant.

The second new index again dealing with F_{max}, is intended to take into account the shape of the curve between t_0 and the maximum point, M, on the graph. Referring to Figure 2, observe that for a given F_{max}, point B represents the limiting best case. Although a curve in practice cannot reach B, it may approach it by rising almost straight upwards then peak at it's maximum, M. But to take into account the shape of the curve, it is not the point M that is of major concern, but rather the closest point on the curve to B. This closest

point is the tangent formed by a ray sweeping clockwise from the force axis until it just touches the curve at the point T in Figure 2. The line joining B and T will intersect line OM at the point S. Observe that for a given point M, the steeper the curve rises, the larger the segment ST. The ratio of lengths ST/SB gives a proportion of the distance to the best case point accounted for by the location of the point T. We now define the adjustment to F_{max} as,

$$ADJF_{max} = \frac{ST}{SB} F_{max} \tag{3}$$

Curves with identical points M and common ratio ST/SB have tangents lying along a line parallel to OM. In this sense $ADJF_{max}$ defines a class of curves each making trade-offs of steepness of rise with sharpness of the turn to reach M. To compute $ADJF_{max}$ requires some software capable of digitizing certain points on the wetting balance curve. An explicit formula for $ADJF_{max}$ suitable for such software is given by,

$$ADJF_{max} = \frac{ST}{SB} F_{max} \tag{4}$$

where,

$$ST = \left[(t_{tan} - x_s)^2 + (F_{tan} - y_s)^2 \right]^{1/2} \tag{5}$$

$$SB = \left[x_s^2 + (F_{max} - y_s)^2 \right]^{1/2} \tag{6}$$

and (x_s, y_s) are the coordinates of point S with

$$x_s = \frac{t_{tan}}{1 + \dfrac{t_{tan}}{t_{max}} - \dfrac{F_{tan}}{F_{max}}} \tag{7}$$

$$y_s = x_s \frac{F_{max}}{t_{max}} \tag{8}$$

The next two new indices employ the theoretical maximum force, $F_{th} = (E + F_b)/p$, where F_b is the buoyant force, p is the perimeter and $E = 0.49$ Jm^{-2} is the surface energy. Define, the third new index

$$R_{max} = (100\%) F_{max} / F_{th} \tag{9}$$

to be the ratio (expressed as a percent) of the maximum attained wetting force to the theoretical maximum wetting force. The fourth new index, which uses F_{th}, is similar to the construction of $ADJF_{max}$

and is the percent to the theoretical best case, $PCTF_{th}$. In Figure 2, $PCTF_{th}$ is the ratio of $S'B'$ to $S'T'$ given as a percent, i.e.,

$$PCTF_{th} = (100\%) \frac{S'B'}{S'T'}. \qquad (10)$$

With the substitution of F_{th} for F_{max} in x_s, the same formula used to calculate SB and ST for $ADJF_{max}$ may be used to calculate $S'B'$ and $S'T'$ respectively.

The fifth new index is simply the range of force values computed as,

$$F_{range} = F_{spike} - F_{min}. \qquad (11)$$

The quantity F_{range} is the only index among the five new indices that incorporates information concerning dewetting.

SECTION III. INDICES AND EXPERIMENTAL TEST COMPARISON

In this section, the new and current indices and wetting balance parameters will be examined with respect to correlation with visual inspection. These new measures are not intended to replace or render obsolete the current indices. Rather, they may be combined with the current indices using discriminant analysis to enhance the predictive power of the wetting balance.

Experimental
  Equipment

Lead finish thickness measurements were made on a Seiko 1575 coating thickness guage, Fig. 3.

Wetting balance testing was performed on a Kester wetting balance Model #KS-110, Fig. 4. Hot solder dip lead finish application was done on a modified Hollis TDL-12 wave solder machine, Fig. 5. Matte tin electroplate lead finish was applied using a 10% H_2SO_4 wren bath with Janus green B, IGEPAL-630 and Hydroquinone as bath additives.

Burn-in was performed on a microtest oven Model #PNC 2-16-5 using dynavision test boards, Fig. 6.

Visual inspection was performed on a Bausch & Lomb stereo zoom microscope.

Experimental
 Method

A total of 322 18 lead ceramic dual in-line packages were sealed
with no die in the packages. These parts were then split into seven
(7) groups of 46 units per group and individually labeled. Each group
was then submitted for lead finish preclean processing per Table
2. Three units were pulled from each group and wetting balance tested
immediately after precleaning using O.A. type flux (use of R type flux
was attempted but the freshly cleaned leads oxidized so quickly during
drying prior to wetting balance testing that the wetting curves
obtained were unuseable). The three unit samples were then visually
inspected @ 10x. The remainder of each group was moved on to either
matte tin electroplate or hot solder dip lead finish application.
After lead finish application, the coating thickness was measured.
Another 3 unit sample was taken from each group and wetting balance
tested using R type flux and subsequently visually inspected @ 10x.
Each group was then split in half. One half of each group was
subjected to a 168 hour burn-in @ 125 C per MIL-STD 883. The other
half of each group was subjected to 424 hours of burn-in @ 125 C.
After burn-in was complete, 3 unit samples were then pulled from each
burn-in subgroup and wetting balance tested using R type flux and
subsequently visually inspected @ 10x. A process flow diagram is given
in Figure 7 for clarity. The test methods compared against visual
criteria are DeVore's solderability index, SI, Wooldridge's test,
MOD202, an industry standard, IS, quoted by Becker, and the
MIL-STD-883C test, TM2022. Section I contains a description of each
test. Table 3 displays test results for the visual criteria of percent
coverage and defect category. From considering number of passing
units, it is apparent that the TM2022 test is most stringent followed
by IS, SI, and MOD202.

There is good agreement on all four tests for predicting high
coverage. Thus, given that a unit passes one of the solderability
tests, there is a high probability that the unit will have at least 95%
coverage. But only test MOD202 identified a large proportion of the 95
- 100% category.

On defect categories there seems to be an inability of the tests
to correctly distinguish between the "No-Defect" and "Asperous"
categories. DeVore's test yielded the highest proportion of passes in
the "No Defect" category. Only the test MOD202 identified a high
proportion of the "No Defect" units correctly. However, this same test
had 72% misclassifications.

It seems that the usual tests for good solderability are not well
suited for detecting defect categories. Yet the tests are strict
enough to usually identify good coverage. In order to be an effective
test for solderability from a visual criteria standpoint, a test should

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be able to both appropriately classify passing units and to pass units from the appropriate categories. To develop other methods of accessing solderability, we turn to quantifying solderability properties using indices, rather than a pass/fail test procedure. The indices considered are DeVore's SI and CW, the stability of wetting, SW, presented by Becker and the five new indices discussed in Section II: $ADJF_{max}$, F_{range}, MAXANG, $PCTF_{th}$ and R_{max}. We will look for correlations among these indices and ultimately for relations to visual criteria.

A principal components analysis on these indices was inconclusive due to approximately equal weighting of each index in the resulting component. However, we do report the Pearson-product-moment bivariate crrelations in Table 3. From these bivariate correlations we see that CW has a strong positive linear relationship with four of the new indices and the index SW. But conclusions about CW are difficult to draw because CW was only able to be computed on 12 or fewer cases. This is due to the difficulties discussed in Section II of observing equilibrium values. The remaining correlations were based on a minimum of 95 observations. Observe that only moderate correlations exist between the other variables so that pairwise redundancy of indices is not indicated. Each indice is providing information on different aspects of the soldering process.

SECTION IV. DISCRIMINANT ANALYSIS

Having described indices in Sections I and II and compared them informally in Section III, we now examine the indices for their ability to classify units according to visual criteria. If a method can be found to use the wetting balance to correctly classify units by visual criteria, then the aforementioned limitations inherent in visual inspection may be avoided. Of course the difficulty in this attempt is apparent in trying to use an objective technique to predict a subjective inspection. Subtle differences on the wetting balance may give no corresponding difference in visual results. Indeed, it may not even be desirable to predict visual results exactly if the visual inspection has a large amount of variability.

The method we use to attempt to classify parts into wide visual categories is discriminant analysis. Discriminant analysis seeks to build a linear combination or discriminant function from several discriminating variables. Coefficients for this function are chosen in such a way that scores from the discriminant function may be used to classify observations into discrete categories, in this case, visual categories. Two activities are addressed by discriminant analysis. First, interpretive use of discriminant analysis provides insight into which variables are best able to discriminate between categories. The second use is for actual classification purpose on the basis of scores

of a discriminant function which most closely resembles those of a particular category. A good introduction to discriminant analysis is contained in reference 7.

It should be stated that many factors may affect the discriminant function derived in this paper. Among these factors may be a type of unit being soldered, flux type, solder composition, equipment, operators and a host of process variables both known and unknown. Consequently the discriminant functions developed here may not be suitable to be transported to another production situation. Appropriate discriminant functions would have to be developed for the process in question. However, the methodology may still be applicable. From the interpretive use of discriminant analysis there may be some value in identifying useful indices and parameters while the classification advantages are more direct.

To begin, the current and new indices set forth in Sections II and III were analyzed via SAS, The Statistical Analysis System Software Package, to obtain a set of indices to be included in building discriminant functions for the visual criteria of solder coverage. Percent coverage was accessed visually on each unit and grouped into the categories: 0-24%, 25-49%, 50-74%, 75-94%, and 95-100%. The selection criteria for the discriminant functions were based on Wilk's lambda and produced the set of indices $ADJF_{max}$, F_{range}, MASANG, $PCTF_{th}$, R_{max}, and SI. Two discriminant functions were judged significant on the basis of a likelihood ratio test.

Table 5 contains the structure coefficients for these indices on the two discriminant functions. The structure coefficients are correlations between the index and the disciminant function. Hence they show the degree of relationship between the index and the function; values near +1 or -1 indicate that the index and the function convey similar information for discrimination between coverages. The raw discriminant function coefficients used to obtain observation scores are reported in Table 5 , but the raw coefficients are not intended for interpretation. Figure 8 shows the classification centroids and boundaries for coverage on the basis of the two discriminant functions developed. Note that 87% (81 or 93) of the observations were correctly classified with these discriminant function.

Using these same variables, a similar procedure was carried out on the defect categories, "No-Defect", "Asperous", "Dewet", "Pinhole", and "Non-Wet". The structure coefficients and raw discriminant coefficients are reported in Table 5. From Figure 9 it is apparant that the categories "Pinhole" and "Asperous" have centroids close together making prediction difficult. Still, 59% (55 of 93) of observations were correctly classified.

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SECTION V. FIELD EXAMPLE AND CONCLUSION

Having developed elaborate discriminant functions in the preceeding section, we will observe the effectiveness of applying these functions on production units. Here 36 units were tested on the wetting balance after completing the standard production flow. The results are that 92% were correctly classified on the basis of coverage and 53% were correctly classified on visual defect categories.

In this paper, several solderability indices have been explored including five new indices. Relations of the known solderability tests, SI, TM2022, MOD202, and IS have been compared to visual criteria. The result is an indication that most of the tests (with the possible exception of Woolridge's, MOD202) are too strict since they perform poorly at identifying most of the parts with good visual coverage. These same tests have difficulty discriminating "asperous" units from "no-defect" units.

An attempt was made to develop discriminant functions comprised of solderability indices and parameters to predict coverage and defect category. These discriminant functions correctly identified 87% of the units for coverage and 59% for defect categories. Besides better discriminating capability, these functions have the added advantage of classifying units into several categories, not just a "pass/fail" choice. Finally these discriminant functions were successfully used on production units to predict both coverage and defect category.

Although some have argued that the wetting balance is more indicative of the symptoms of poor solderability than the cause (reference 1), we believe that through the use of the wetting balance prediction techniques can be employed to generate functions which produce parameters that can be monitored in a real time SPC program during production component tinning. In this way an alert may be given so that corrective actions can be executed and causes may be explored.

Even though wetting balance measurements may not have reached their full potential, benefits from the use of indices and discriminant analysis methods may be realized.

Wetting Balance Test or Indice	Criteria	Source	Reference
Solderability Index	$SI = \dfrac{F(2)}{t_0(F_{spike} - F_{end})}$ pass if $SI > 5$	DeVore	2
Coefficient of Wetting	$CW = F_{eq}/t_{eq}$	DeVore	3
Modified MIL-STD-202 Method 208	MOD202: pass if $\begin{cases} t_0 \le 1 \text{ sec and} \\ F(2.5) \ge 200 \text{ }\mu N/mm \text{ and} \\ F(5) \ge 200 \text{ }\mu N/mm \end{cases}$	Woolridge	5
MIL-STD-883c TM2022	TM2022: pass if $\begin{cases} t_0 \le 0.6 \text{ sec and} \\ F(1) \ge 2/3\, F(5) \end{cases}$		6
Industry Standard	IS: pass if $F(2) \ge 300 \text{ }\mu N/mm$	Becker	4
Stability of Wetting	$SW = F_{max} - F_{end}$	Becker	4

TABLE 1. Current Solderability Tests and Indices

GROUP	ORIENTATION	TIME
1	stacked	4 min.
2	singulated	2 min.
3	singulated	1/2 min.
4	no clean	
5	singulated	4 min.
6	stacked	2 min.
7	stacked	1/2 min.

Table 2. CLEANING METHOD (50% H_2SO_4 @ 90-100 C)

COVERAGE

TEST	CATEGORIES 75-94%	95-100%	TOTAL PASSING	PERCENT OF PASSES IN 95-100%	PERCENT OF 95-100% IDENTIFIED
SI	0	24	24	100	32
SW	0	21	21	100	28
TM2022	0	6	6	100	8
MOD202	5	56	61	92	74

DEFECTS

TEST	CATEGORIES NO-DEF	ASPEROUS	DEWET	NON-WET	PINHOLES	TOTAL PASSING	PERCENT OF PASSES IN NO-DEF	PERCENT OF NO-DEF IDENTIFIED
SI	8	15	1	0	0	24	33	36
SW	4	14	1	0	2	21	19	18
TM2022	0	4	1	0	1	6	0	0
MOD202	17	31	2	0	11	61	28	77

TABLE 3. RESULTS OF SOLDERABILITY TESTS
BY VISUAL COVERAGE AND DEFECT CATEGORY

	CW	SI	SW	ADJFmax	Fmax	MAXANG	PCTFth	Rmax
CW		0.51	0.81	0.81	0.81	0.89	0.87	0.10
SI	0.51		0.19	0.37	0.22	0.62	0.56	-0.07
SW	0.81	0.19		0.05	0.16	0.38	0.46	-0.27
ADJFmax	0.81	0.37	0.05		0.60	0.23	0.80	0.60
Fmax	0.81	0.22	0.16	0.60		0.48	0.80	-0.02
MAXANG	0.89	0.62	0.38	0.23	0.48		0.65	-0.29
PCTFth	0.87	0.56	0.46	0.80	0.80	0.65		0.02
Rmax	0.10	-0.07	-0.27	0.60	-0.02	-0.29	0.02	

TABLE 4. CORRELATIONS AMONG INDICES

COVERAGE

	STRUCTURE COEFFICIENTS		RAW COEFFICIENTS		COVERAGE CATEGORY	NO. OF CASES	CORRECTLY CLASSIFIED
	FN1	FN2	FN1	FN2			
SI	0.537	-0.210	0.009	-0.139	25-49%	2	100%
PCTFTH	0.854	-0.360	-0.065	-0.094	50-74%	11	91%
MAXANG	0.761	0.225	1.380	2.373	75-94%	13	38%
ADJFMAX	0.749	-0.108	0.029	0.033	95-100%	67	96%
BESTFTH	-0.471	0.385	-0.044	-0.021			
FRANGE	0.792	-0.432	0.009	-0.007			
					TOTAL NUMBER	93	81

DEFECTS

	STRUCTURE COEFFICIENTS		RAW COEFFICIENTS		DEFECT CATEGORY	NO. OF CASES	CORRECTLY CLASSIFIED
	FN1	FN2	FN1	FN2			
SI	0.464	0.388	0.098	-0.032	NO-DEF	20	45%
PCTFTH	0.770	0.371	-0.028	-0.035	ASPEROUS	42	74%
MAXANGLE	0.192	0.815	-0.833	2.473	DEWET	4	50%
ADJFMAX	0.835	0.355	0.025	0.012	PINHOLE	19	47%
BESTFTH	-0.358	0.026	-0.054	0.041	NON-WET	8	75%
FRANGE	0.752	0.194	0.007	0.001			
					TOTAL NUMBER	93	57

TABLE 5. DISCRIMINANT ANALYSIS COEFFICIENTS
AND PERCENT CORRECTLY CLASSIFIED

FORCE

TIME (sec)

BUOYANCY
LINE
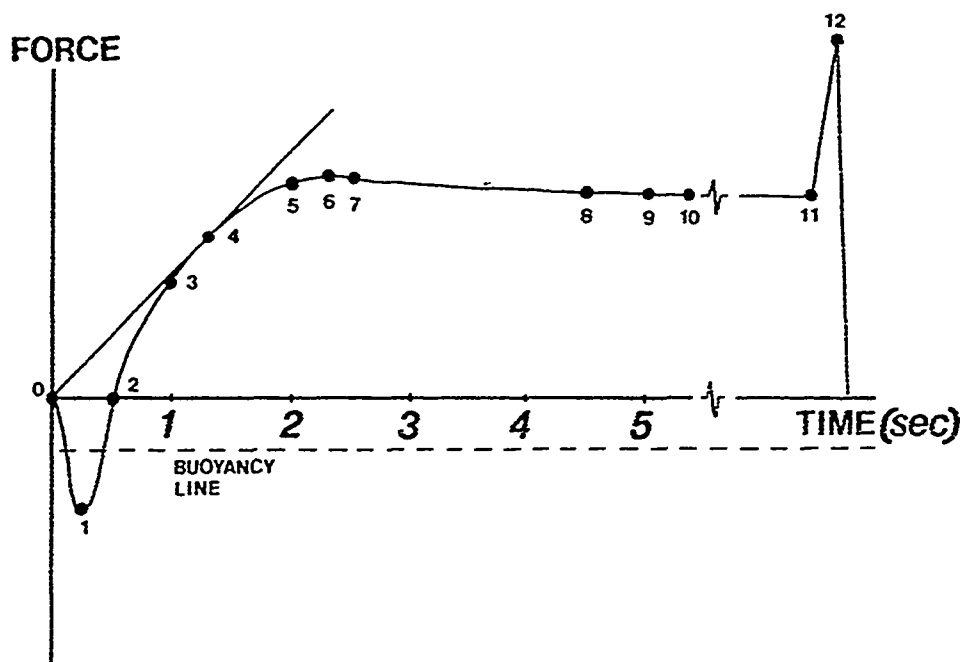
0 - ORIGIN	= (0,0)	7 - t=2.5 sec	= $(t_{2.5}, F_{2.5})$
1 - MIN	= (t_{min}, F_{min})	8 - t=4.5 sec	= $(t_{4.5}, F_{4.5})$
2 - t_0	= $(t_0, 0)$	9 - t=5 sec	= (t_5, F_5)
3 - t=1 sec	= (t_1, F_1)	10 - EQUILIBRIUM	= (t_{eq}, F_{eq})
4 - TANGENT	= (t_{tan}, F_{tan})	11 - END	= (t_{end}, F_{end})
5 - t=2 sec	= (t_2, F_2)	12 - SPIKE	= (t_{spike}, F_{spike})
6 - MAX	= (t_{max}, F_{max})		

FIGURE 1. WETTING BALANCE PARAMETERS
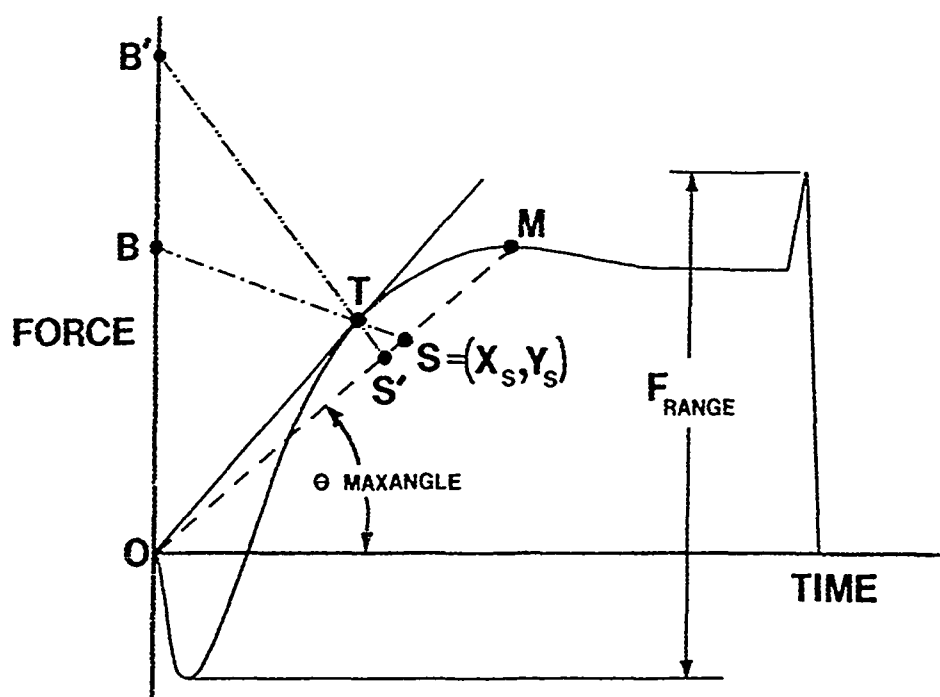
FIGURE 2.   POINTS USED TO CALCULATE NEW SOLDERABILITY INDICES
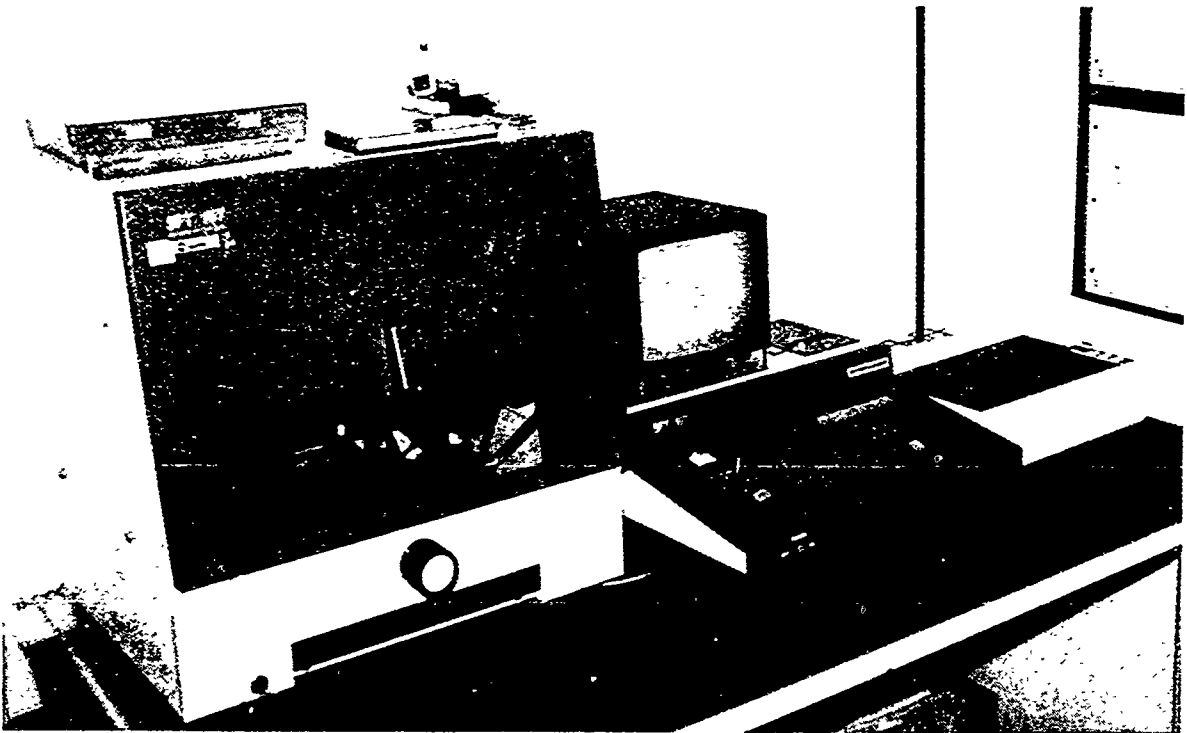
FIG. 3.   Seiko 157S X-ray Fluorescence Coating Thickness Measurement Guage
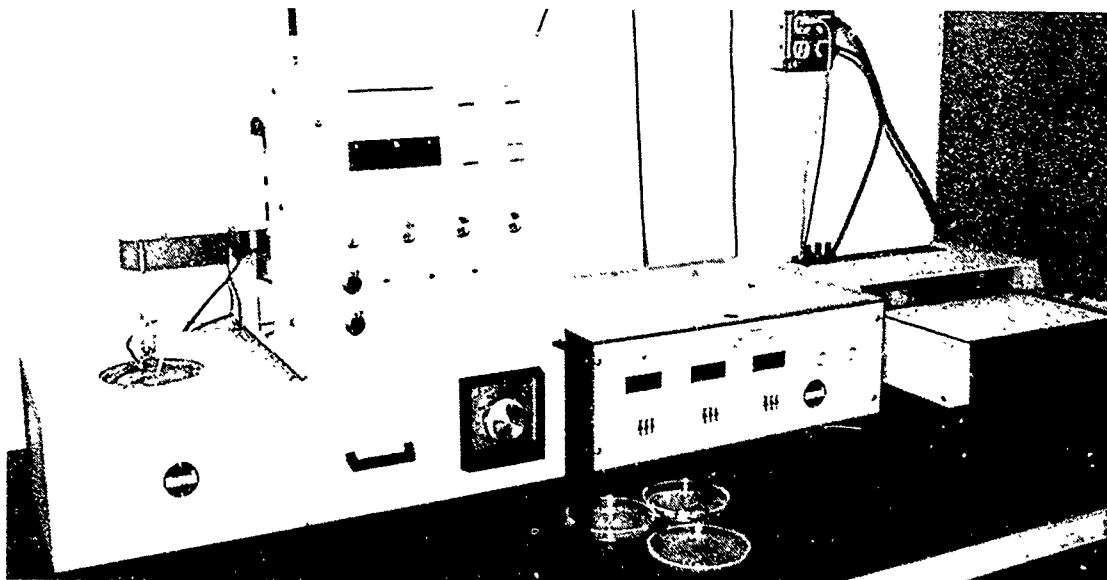
FIG. 4   Kester Wetting Balance Model #KS-110
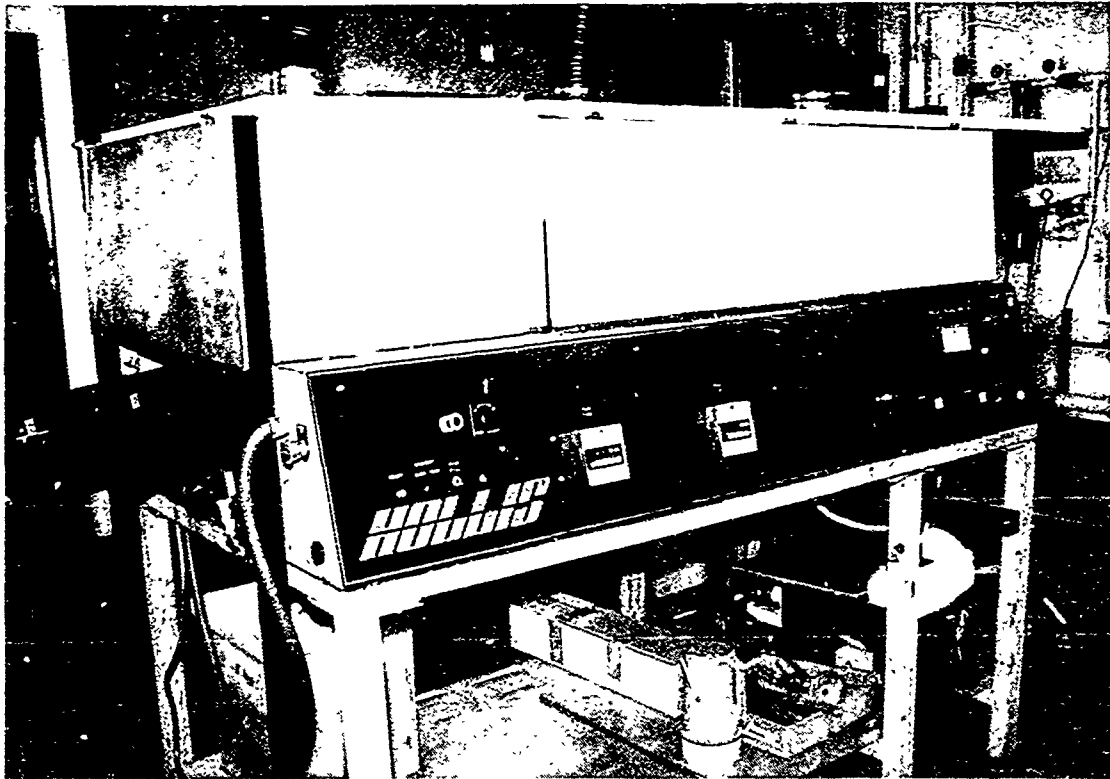
FIG. 5 Hollis TDL-12 Wavesolder Machine

FIG. 6. Microtest Burn-in Oven
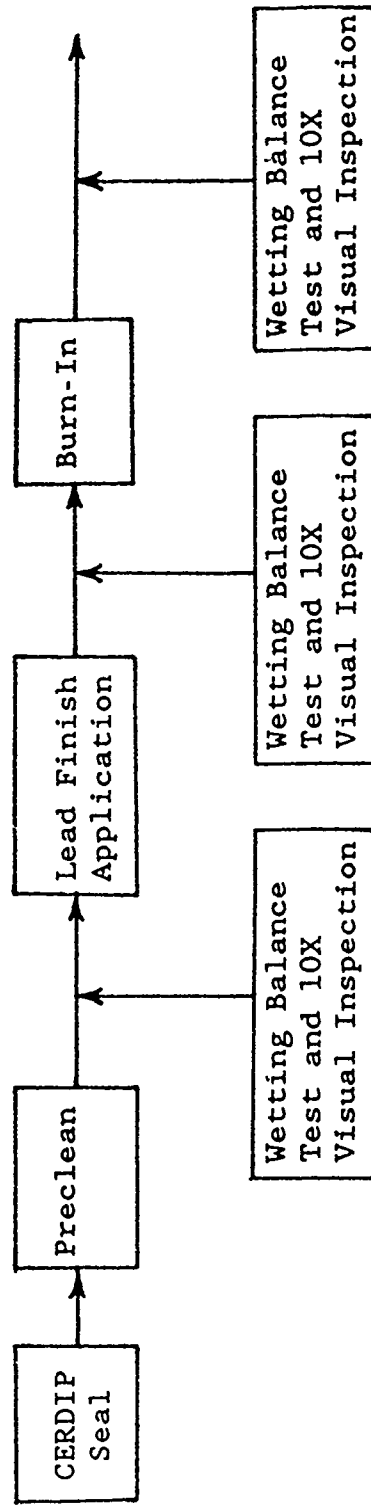
FIGURE 7. EXPERIMENTAL PROCESS FLOW DIAGRAM
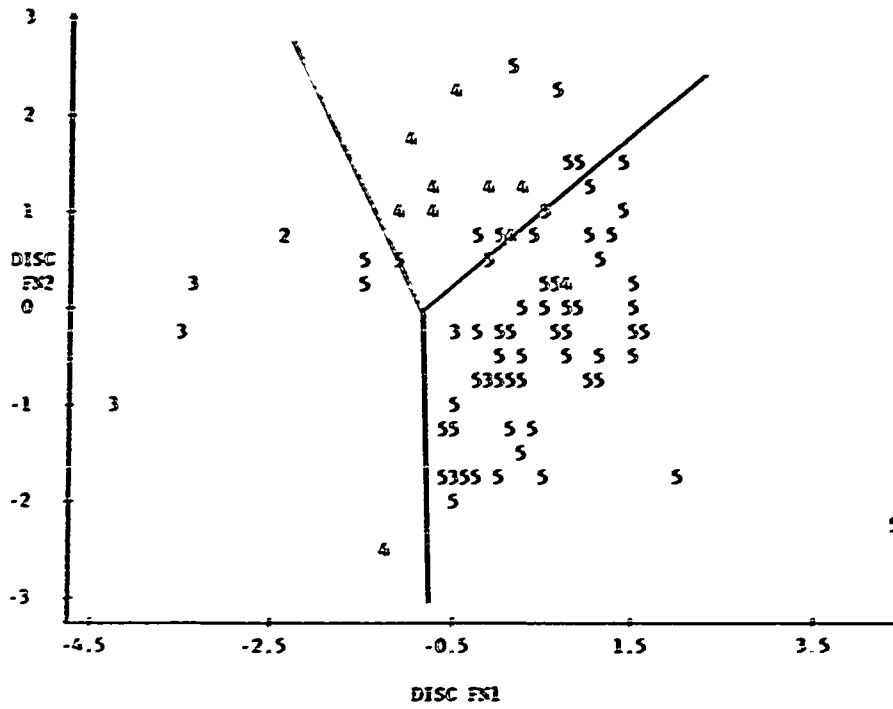
FIGURE 8. PLOT OF DISCRIMINANT FN1 VS DISCRIMINANT FN2 FOR COVERAGE
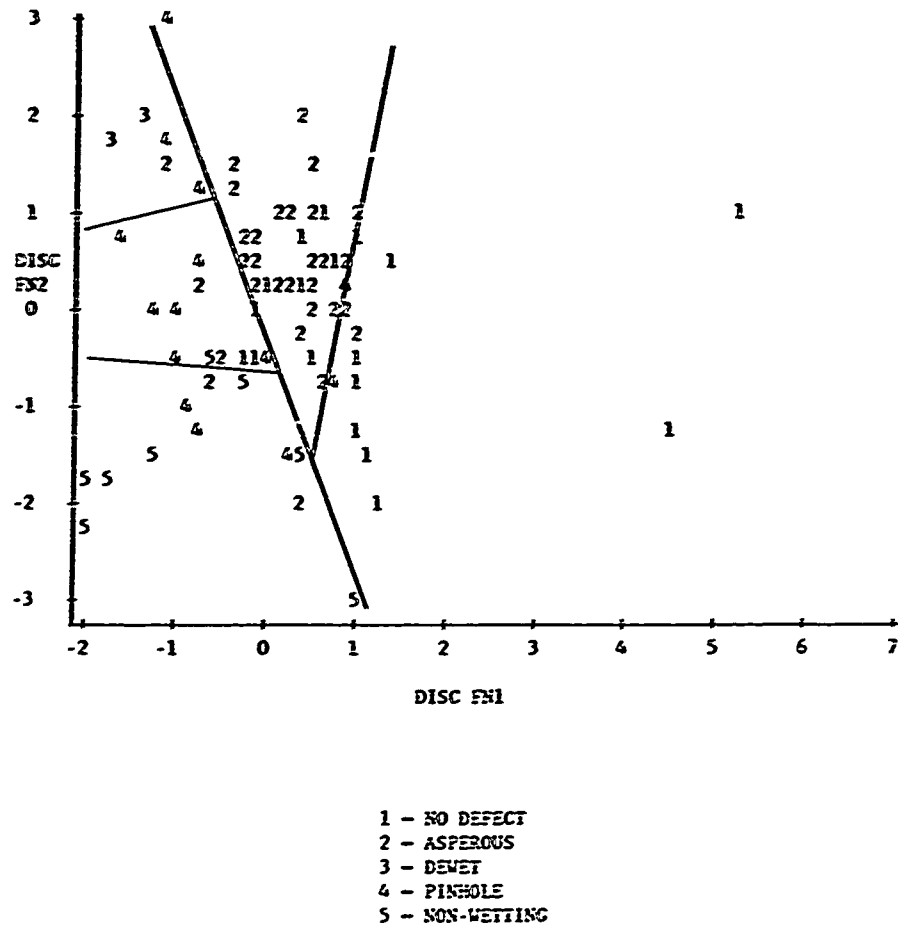
FIGURE 9. PLOT OF DISCRIMINANT FN1 VS DISCRIMINANT FN2 FOR DEFECTS

REFERENCES

1. DeVore, J. A. "The Mechanisms of Solderability and Solderability Related Failures." Printed Circuit World Convention III. (May 1985) IPC Technical Review. (Feb. 1985): 17-20.

2. DeVore, J. A. "Solderability and Surface Mounting." 12th Annual Soldering Technology Seminar Proceedings. China Lake Naval Weapons Center. (Feb. 1988): 301-313. NWC TP 6896, EMPF TP0003.

3. Wild, R. N. "Some Component Lead and Solderability Issues." Brazing & Soldering No. 9. (1985): 5-10.

4. Allen, B. M. "Testing SMDS For Solderability." Surface Mount Technology. (Oct. 1988): 17-18.

5. Becker, G. "Solderability Testing of Surface-Mount Devices." Electronic Packaging and Production. (Oct. 1987): 32-35.

6. Wooldridge, J. R. "Lessons Learned During a Year of Production Solderability Testing with a Wetting Balance." 12th Annual Soldering Technology Seminar Proceeding - China Lake Naval Weapons Center. (Feb. 1988): 485-496. NWC TP 6896, EMPF TP000.

7. Klecka, W. R.. "Quantitative Applications in the Social Sciences." Sage University Paper Series. (1980): 07-019.

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RECENT COMPONENT SOLDERABILITY
TEST ENHANCEMENTS

by

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ABSTRACT

Critical parameters of the MIL-STD-202 Method 208 and MIL-STD-883 Method 2003 component solderability tests were determined from laboratory experiments. Among the variables examined were steam ager atmosphere, steam ager water quality, component drying, flux quantity, static versus wave pots, and visual inspection variability.

The test results indicate one of the most important variables is steam ager atmosphere. This was evaluated by vapor temperature vs metal coupon weight gain. Other critical parameters are the drying process and inspection method.

Experimental data for some parameters suggest needed changes to the relevant Military-Standard test methods. These changes are proposed based on the experimental work presented, and would improve correlation of solderability test results between suppliers and users.

INTRODUCTION

During the past two years, Texas Instruments Defense Systems & Electronics Group has worked extensively to improve the quality of the lead finishes procured for use in its various assemblies. This effort was carried out through an intensive round of meetings with component suppliers.

This team approach has paid back tremendous dividends. The various quality improvement teams have solved many problems through the systematic application of metallurgical methods and examination of microstructural data. Many component manufacturing process improvements have resulted and have since been validated through increased incoming solderability test yields.

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While working with its suppliers, TI also performed an extensive review of the procedures used at Incoming Test. Both the techniques and the test equipment were compared to the state of the art, Military-Standard Solderability Test Methods (i.e., MIL-STD-883C, Notice 7 Method 2003.5; and MIL-STD-202F, Notice 9 Method 208F), and to what was learned by the quality improvement teams.

However, throughout this time, problems have been encountered in correlating test results. Solderability test results at different locations often differed, even though the same Military-Standard test procedures were used. Therefore, a series of laboratory experiments were performed to help identify the source of the test variability. Six test parameters were chosen for further study: the steam ager atmosphere conditions, the quality of the steam ager water, the drying method following aging, the flux quantity used, the static versus flow solder dip process, and inspection repeatability. These six parameters are the subject of this paper.

STEAM AGER ATMOSPHERE CONDITIONS

During our meetings with suppliers, it was noticed that there was a wide variety of steam aging equipment in use. Some companies used the traditional glass beakers; some with no lid area open, others with a 12% opening. Another set of companies used a number of different steam aging tanks, some produced in house, some commercially available. It was also at this time that Texas Instruments Defense Systems and Electronics Group (TI-DSEG) Incoming Test obtained one of the wide range of commercially available tanks, in this case the Mountaingate Engineering Model ST-200. (See Figure 1.)

Note: The contents of this paper imply neither a direct, nor an indirect recommendation regarding any commercially available equipment.

This equipment variation has resulted in part from the fact that the two Military-Standards do not describe the steam aging equipment in precisely the same way. During aging, MIL-STD-202 states that the parts should be suspended 1-1/2 to 2-1/2 inches from the surface of the water. MIL-STD-883 only specifies a minimum of 1-1/2 inches. In addition, while both standards do state that the lid should cover "approximately" 7/8 of the opening, this has been interpreted by some companies as a minimum, and by others as an exact measurement.

Conventional wisdom was that the temperature and humidity over the water inside a container should be fairly uniform at a given altitude. The humidity was assumed to be at saturation. Perhaps this affected how the test was developed. The types of equipment being used became more diverse, and this raised questions as to whether the conditions really were the same in each type of steam aging equipment.

The experimental work began with measurements on the steam atmosphere. While temperature was easy to measure, directly measuring the humidity inside the chamber proved futile. None of the hygrometers used (wet sock, resistive polymer, or chilled mirror) were effective in the range of humidity found in the ager. To completely characterize conditions in the ager, a technique was needed to monitor ager conditions indirectly.

Therefore, an experiment was developed using an indirect measure of the conditions in the agers: the oxidation rate of copper foil coupons, as indicated by overall weight gain. Copper was chosen in the first test because it oxidized rapidly. Foil coupons were used because the surface area was maximized. The scale used was accurate to +/- 10 micrograms.

This first test measured the oxidation of the copper coupons at different temperatures in the same ager. The nominal size of the coupons was 3 inches X 1.5 inches X 5 mils. Six coupons were conditioned by placing them on end and aging them for 8 hours. The test was repeated at six different temperatures (80C, 85C, 90C, 95C, 98C, and 100C). The temperature was measured at the component level in the center of the chamber and recorded. The average weight gain for all the coupons at each temperature was then calculated, as shown in Figure 2.

The data formed a pattern which we have seen repeated many times. The pattern has been confirmed in subsequent work at other companies. The weight gain increases from 80C to a peak near 95C and then decreases rapidly to no measurable oxidation at 100C.

This result was initially a surprise, but could have been anticipated. The vapor pressure of water in air is known to increase as the temperature increases (Table 1). At 100C and 100 percent relative humidity, the air is 100 percent water vapor. This excludes the oxygen and other gases in the ambient air. In order for the copper to oxidize, it is necessary for three components to be present: the copper coupon, water vapor and oxygen (Reference 1). As the oxygen content in the air decreases, the oxidation rate decreases. When the steam agers are operated near 100C, almost no oxidation occurs.

This lack of oxidation was confirmed by both the weight gain and the visual appearance of the coupons. After 8 hours of steam at 100C, the copper coupons appeared as though they were not aged at all.

In summary, from 80C to approximately 95C, increasing the temperature increases the rate of oxidation. Above approximately 95C, the oxidation rate begins to decrease apparently due to a decreasing oxygen level. In a laboratory ager, the level of oxidation increased by a factor of 100 (i.e. 10,000 percent) as the temperature dropped from 100C to 95C.

A second test was performed, this time using 63-37 tin-lead solder foil coupons in place of the copper. All other aspects of the test were kept constant. (See Figure 3, which shows the average weight gain for the tin-lead coupons). The pattern of the data repeated that shown for copper in Figure 2, but at a much lower overall weight gain. This evidence confirms that the same factors are controlling the rate of oxidation for both copper and solder.

A third test compared the relative repeatability of the steam aging test when performed in different agers. Five agers were tested, four were Mountaingate models (two were 5 drawer sizes, two were 3 drawer sizes). The fifth ager was a 2000 ml beaker on a hot plate. The agers were set to operate at 87 +/- 2C. Six coupons were placed in each, again standing on end, for 8 hours. This test was performed at Incoming Test during normal production conditions. The resulting average weight gains are shown in Figure 4, and summarized in Table 2.

This data indicates that there was a significant difference in the amount of oxidation observed in different agers. The largest variation was between MG3 and MG4 with an 82 percent difference in weight gain. (MG2 was not tested). The next largest variation was between MG5 and MG4, and was 76 percent. As can be seen in Table 2, the variation of results within each ager was also very high. This indicates that an additional factor was influencing the test result.

To explore this additional factor further, a fourth experiment was performed. Six copper coupons were aged in each of the five Mountaingate agers. This time however, the test was performed under more controlled conditions. Each of the agers was continuously monitored to insure that it was not disturbed and that the temperature was always at 87 +/- 2C.

The results are shown in Figure 4A and Table 2. Again the variation between the highest ager (MG1 or MG3) and the lowest (MG4) is fairly high, 86 percent. However, this variation is minute when compared to the 10,000 percent variation found when ager temperature is allowed to change. The residual variation might be due in part to the ager set-up: MG4 was the only ager with a perforated platform between the steam and the drawers. This might have affected the flow of steam to the components. The other agers contained no platform. Among the "no platform" models, the results are very close, all within 13 percent. Also, coupon-to-coupon variation within each ager, is also much smaller when conditions are more controlled.

The results of these comparison tests indicate that the oxidation rate of parts within the ager is very sensitive to small variations in conditions. In order to get consistent test results, the aging equipment, and it's operations must be very carefully controlled. These controls have been incorporated into the TI-DSEG Incoming Test procedures. While variations between the steam aging equipment as described by Mil-Std-202, versus Mil-Std-883 should be eliminated, it appears that the most significant factor, leading to inconsistent steam aging, results from the fact that neither specification defines vapor temperature.

This data has been confirmed by suppliers. For example, one large resistor manufacturer was consistently passing the solderability test at its own factory but failing at TI. A three month average showed a 32% reject rate at TI.

After discussing the importance of steam temperature with the supplier, the supplier's factory quickly found that its ager was operating at 99 to 100C. This was lowered to 95C, and the tests repeated. They found that their new reject rate increased to slightly above the reject rate at TI. This resulted in a much closer correlation of results. Most importantly, in-house feedback with the corrected steam temperature, helped the supplier to develop an improved solderable lead finish.

AGER WATER QUALITY

Current versions of Mil-Std-202 and Mil-Std-883 allow for the use of either distilled or deionized water in steam aging. However, some suppliers still challenge the use of deionized water in the steam agers at Texas Instruments. Furthermore, although distilled or deionized water is specified, no requirement is specified as to a measurable parameter of water quality.

This issue of DI versus distilled water is important because
DI water is fairly inexpensive to produce and is more readily
available at most manufacturing facilities. Distilled water is
generally less readily available. Also several grades of each
water can be obtained.

Given the concern of component part suppliers, a test was
performed to determine if there might be a significant variation in
the solderability test results due to the type of water used.

Two Mountaingate steam agers were set up and operated at 87
+/-2C. One was filled with 8 megohm DI water; the other with
distilled water. Seventy-two, 13 piece sample lots were then aged
in these two units. Half the samples (6 parts) were aged over the
DI water; the other half (7 parts) over the distilled water.

The usual dip-and-look test was performed in accordance with
the Military-Standard test methods. Pass/fail data was recorded.
Failure was defined as one lead out of either six or seven parts
having less than 95% acceptable solder coverage.

The results of the test are summarized in Table 3. All
results are identical except for 2 lots of discrete semiconductors,
which failed in the distilled water but not in the DI water. This
would indicate that the type of water used has no significant
impact on overall solderability test results. However, no attempt
was made to test all possible grades of distilled and deionized
water.

DRYING CONDITIONS

The major Military-Standards do not address how the parts are
to be dried following steam aging. There are several methods
commonly in use. Some companies let the samples air dry. The drying
times vary from 10 minutes to 24 hours. Other companies use ovens
set from 50 to 100C for much shorter periods of time. Still others
use heated blow dryers.

Alcohol vs Air dry - A new and novel drying procedure
recently was mentioned in a proposed revision to MIL-STD-202. This
new method would involve a 10 minute immersion of the wet part in
isopropyl alcohol (IPA), followed by a 10 minute air dry. The water
dissolves in the alcohol, the alcohol then evaporates very quickly
from the body of the part.

A test was performed to assess what affect the alcohol dry might have on solderability test results. Fifty dual-in-line package integrated circuits (DIP ICs) were obtained. All were from one manufacturer and had the same part number and date code. All had alloy 42 lead frames with a solder dip finish. All were aged in DI water for 8 hours at 87 +/- 2C. Twenty-five of the parts were then dried by immersing them for 10 minutes in IPA, and drying in ambient air for 10 minutes. The other 25 parts were dried for 120 minutes in the ambient air without an IPA dip. Both sets of parts were then solder dipped and inspected using the normal MIL-STD-883 procedure.

The results are shown in Table 4. The "observations" are classified into two categories of a greater than 5% defect area: 1) surface roughness, and 2) dewet/nonwet. Dewet and nonwet are defined in the Military-Standards. The surface roughness usually appears as a roughened patch of solder that is found on some manufacturer's parts following steam aging and solderability testing. It commonly looks like dewet except that it is only on the surface, with an adequate solder layer underneath. At the present time, surface roughness is not defined to be a defect in the Military-Standards, but it is an item of concern because it is difficult to distinguish it from defined defects with a visual inspection.

The data shows that the incidence of both types of observations is much higher on the parts that are air dried for 120 minutes. The parts that were dried in IPA looked much better following the solder dip. This indicates that the IPA drying cycle does affect the results of the solderability test in a way that is significantly different than an air dry. This data could also indicate that the surface roughness is related to a contaminant on the lead finish.

The difference in these test results is apparently due to the cleaning action of the IPA. Soluble contaminants are cleaned off the leads prior to solder dip. Therefore, this drying method is, in reality, a cleaning method which should not be allowed in the Military-Standard, because it could create a major change in test results.

Drying times - Since the Military-Standards provide no instructions on how to dry components following steam aging, recent proposed revisions have included some guidelines on drying time. Usually these guidelines provide a maximum time limit allowed prior to dip, but do not specify a minimum time.

In order to help provide guidance on an adequate minimum drying cycle, a test was performed to determine how much time a part required to dry following steam aging.

Three different samples were used: a 1.5 inch square piece of Sn-Pb plated copper foil, 6 RJR trimpots, and two 28 pin DIP-ICs. Each was weighed prior to the test, and then at regular intervals following steam aging. The scale used was accurate to +/- 10 micrograms.

The results are shown in Figure 5. The copper foil dried most quickly, in approximately 1.75 hours. The trimpots dried in approximately 3 hours and the ICs in 5 hours.

There were still readily measurable levels of moisture on dip ICs after 4 hours of drying under certain ambient conditions. This is important because these devices appear to be dry after only 10 to 15 minutes. In order to assure complete reproducibility of solderability test results, it may be necessary to allow the parts to reach some level of dryness prior to solderability testing. It appears that a new revision to the Military-Standards should include a minimum air dry time. Defining that minimum air dry time will require further testing.

FLUX QUANTITY

An interesting item was discovered during testing of several other process variables and concerns the amount of flux on the leads when dipping in the solder pot.

Both Military-Standards state that the part shall be immersed to within 0.050 inches of the part body, or to the effective seating plane.

A test was performed on two groups of 50 DIP-ICs. Both groups were steam aged for 8 hours, then mounted in a dipping fixture. The first group was dipped with a carefully controlled flux level, at 0.050 inches from the body. The other group was intentionally dipped excessively, past the tops of the leads. This allowed flux to become trapped in the dipping fixture . Both groups were then processed through the usual Military-Standard solderability test.

When the inspection was complete it was found that 11 of the 50 parts in the over-fluxed group failed for apparent dewets, while none of the parts in the control group failed. A photograph of the apparent dewets on an over-fluxed part is shown in Figure 6. When redipped, these dewet areas completely disappeared.

These results confirmed previously published data (Reference 2) that reported excessive flux applied to the part continued to vaporize throughout and after the solder dip, causing the solder surface to be disturbed.

The solderability test can be improved. The Military-Standard test methods should be changed to state that devices used to hold the parts, while dipping in the flux and solder baths, shall be designed to avoid any excess flux trapped in the fixture.

SOLDER DIPPING

Another difference between the solderability tests specified in the Military-Standards is the type of solder pot that is to be used. MIL-STD-202, in paragraph 2.1, specifies a static solder pot. MIL-STD-883, in this same paragraph, allows either a static or flowing pot.

A test was performed to determine if there was any significant difference between the solderability reject rates obtained from a flowing versus a static pot.

A test matrix was constructed. Representative samples were selected, from all the most common lead metallization systems, including gold over nickel, and gold over copper connectors; and tin-lead over nickel, and tin-lead over copper axial passive components. Also included were tin-lead over alloy 42 IC leads, and gold-plated nickel lead finish for discrete semiconductors.

Samples of each lead metallization system were tested in two different areas, a regular Incoming solderability lab and a pretinning shop. (The pretin area served as a control). The test conditions used at the Incoming area were the normal solderability test parameters: 245C, SN63 solder and R flux. The pretinning shop used 260C, SN63 solder and RMA flux. Steam aging was performed in both areas: 8 hours for ICs and 1 hour for the other parts. At Incoming, parts were tested with both static and flowing pots, while the pretin area used only a flowing pot.

The test was performed on test groups consisting of 90 samples of each gold plated part, and 30 of the other parts. Separate test groups were tested in each of the solder pots in each of the test areas. Each part type consisted of one part number from one manufacturer and one date code. After the solder dip, each part was inspected and pass/fail data was recorded.

The data is compiled and summarized in Table 5. For each pot, the total number passed and failed is shown for each part type.

The over-all totals at the bottom of the table show that the static pot at Inccming failed a few more parts, at 20 percent, than the flowing pot at 13 percent. Despite the RMA flux, the pretin shop failed a surprisingly large 12 percent of the same parts.

The high percentage of the failures at the Pretin Shop was due to a problem with the gold plate over copper connectors. In this type of connector, the copper is a barrier plate layer between the gold and the underlying beryllium copper connector pin. When pretinning these connectors, if the copper plate is not thick enough, it will dissolve from the high temperature and agitation in the flowing pot, exposing the unsolderable beryllium copper below. TI usually requires a layer of nickel plating between the beryllium copper and the gold. This nickel barrier layer, which is typically verified by X-ray fluorescence (XRF) or microsectioning, prevents this type of problem from occurring. Where nickel plating is not practical, a thick copper plate is specified instead.

Another interesting observation, but one which has no ready explanation is that the flowing pot failed slightly more gold plated connectors than did the static pot. This result is confirmed by other Incoming solderability test yields, and may be due in part to the dynamics of the wave in a flowing pot on multileaded devices.

In summary, these results indicate that the type of solder pot used might make some slight difference in solderability test results, but other variables probably have a more marked effect.

INSPECTION REPEATABILITY

At the present time most solderability testing is performed by the dip-and-look methods specified in MIL-STD-202 and -883. Each of these tests consists of two processes. The first is the steam age, flux and solder dip process. This creates the lead surface finish which is subsequently inspected . Variations in this process will cause variations in the dipped solder surface. Several of the variations have been discussed in this paper.

The second process is the inspection step itself. This is a separate process, and its purpose is to correctly interpret the true condition of the lead following the solder dip. Just as there are variabilities in the aging and dipping process, there are also variabilities in the inspection step.

The inspection process is independent of the dipping process. It affects the outcome of the test but does not actually change the surface finish itself. In order to achieve a truly reproducible and accurate solderability test, it is necessary to understand and minimize the variables in both processes.

The solderability test inspection is usually performed by specially trained inspectors. One of the most comprehensive and best training programs is the WS-6536 inspector certification program sponsored by the Naval Weapons Center (NWC).

Most routine production type solderability tests are performed visually under stereo microscopes by inspectors who compare the lead condition to their own internally calibrated standard for 95 percent solder coverage. Some companies provide special training aids or reference guides, but the final decision is left to the inspector's judgment. Measurements of defect area are very time consuming and are not used on an ongoing basis.

Given the subjectivity of the inspection process, a test was performed to determine how closely inspectors can visually judge the percent coverage on a part, and to help judge the repeatability of the inspectors' estimates.

Twenty-five parts were selected for this test. All were axial type components, with round leads. All were "marginal" parts, not clearly good or clearly bad. These parts were examined repeatedly by each inspector using the same stereomicroscope and fluorescent ring light each time. The inspections were carried out at 10X magnification with an optical resolution of 66 lines/mm.

The inspectors who volunteered for the test were NWC certified. Two of the inspectors were Category C, one was Category D. Each inspector looked at each lead four times over a period of several weeks. No measurements were taken, no special aids were used. The samples were renumbered in between each inspection, to prevent memorization of sample serial numbers.

The inspectors were instructed to record their estimates of the actual solder coverage on each lead. After all inspections were completed, the range between the highest and lowest estimates on each lead by each inspector was calculated. Several companies participated in this study.

The repeatability data is summarized in Figure 7, which shows a histogram of the difference between the highest and lowest coverage estimate for each lead, and for each inspector. This plot indicates how closely each inspector can repeat an estimate of lead coverage.

The distributions of each inspector in the histograms are approximately normal. The mean for each inspector however, differs by a significant amount. Inspectors A and B were Category C, and their estimates varied by 2 and 6 percent, respectively. The Category D inspector's estimates varied by 18 percent. Three other non-certified inspectors were shown 10 parts each and had estimates that varied by an average of nearly 50 percent.

These results indicate that a well-trained inspector can estimate actual coverage with the unaided eye with a repeatability of about 4 percent. With the pass/fail guideline at 5 percent maximum, this means that on marginal parts, the inspector is to a large degree guessing.

These results point out the continued need for excellent training, and good equipment and above all, some method of measuring the actual size of the defects and calculating percent coverage on marginal parts. The unaided human eye, however well trained, is not able to estimate solder coverages closely enough to make accurate pass/fail decisions without some help. A stage micrometer or grided reticle are both excellent for this purpose and are used at TI. On marginal lots, these aids should be used on the worst lead to calculate coverage.

CONCLUSION

During the past two years, TI and its suppliers have worked aggressively as a team to improve the quality of lead finish solderability. But throughout this time, a recurrent series of correlation problems has been noted in the test results. These correlation problems exist for many categories of component types and lead finishes.

Through the laboratory experiments and process verifications reported in this paper, it has been determined that several critical material and process parameters in the existing Military-Standard solderability dip-and-look test methods can be better defined.

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Here are the major conclusions of the experiments, stated in the context of the need to enhance some aspects of the Military-Standard test method for component solderability:

o   The temperature of the vapor inside the steam agers has a marked effect on the rate of oxidation of the leads. In order to make the test more repeatable, we recommend an 85 to 90C (or 10 to 15 degrees below the boiling point of water) temperature should be specified in the Military-Standards as measured at the component level.

o   Small variations in the steam ager's vapor temperature during the test also have an effect. The standards should state that the 8-hour steam aging should be uninterrupted.

o   Alcohol drying of components following steam aging allows for cleaning of the leads and therefore should not be incorporated in Military-Standards.

o   Although parts look dry only 10 minutes after steam aging, appreciable water still adheres to the lead surface. The standards should be changed to call out a minimum as well as maximum drying time.

o   New data confirms the previously reported deleterious effect of excessive flux. Devices used to hold the parts, while dipping in the flux and solder baths, should be designed to avoid any excess flux trapped in the fixture.

o   Highly trained inspectors, with the unaided eye alone, judge the actual percent coverage on marginal leads with a repeatability of only 4 percent. Measurements must be taken on the worst lead from each marginal test lot, and the coverage calculated.

Despite its many years of use, the dip-and-look test has not yet been fully optimized. As long as these deficiencies remain, this test will continue to yield ambiguous results.

It is only when the test has been optimized that it will be possible to obtain identical results when identical parts are tested at different facilities. It is only then that the true effects of component manufacturing process improvements can be gauged, lasting improvements in lead finishes can be made, and

weapons systems failures can be reduced (Reference 4). Looking beyond the solderability test itself, there still exist further technology gaps in solderability that also must be studied using the scientific method. Areas such as mechanisms, reactions, reaction rates and interfacial energies are all good candidates.

ACKNOWLEDGEMENTS

REFERENCES

1.   Fontana, M.G., Corrosion Engineering, 3rd Edition, McGraw-Hill, New York, 1986, pp. 13-38.

2.   Slay, B.G., "Lessons Learned in Testing Solderability of Integrated Circuits Using Method 2003 of MIL-STD-833," 11th Annual Electronics Manufacturing Seminar Proceedings, NWC TP 6789, Naval Weapons Center, China Lake, CA, February, 1987, pp. 534,535.

3.   Weast, R.C., ed., CRC Handbook of Chemistry and Physics, 62nd Edition, CRC Press, Boca Raton, FL, 1981, p. D-168.

4.   Fazekas, D.A., "Report of the Fleet Hardware Assessment Project -A Survey of the Soldering Problems Observed in Navy Weapons Systems," 11th Annual Electronics Manufacturing Seminar Proceedings, NWC TP 6789, Naval Weapons Center, China Lake, CA, 1987, pp. 75-85.
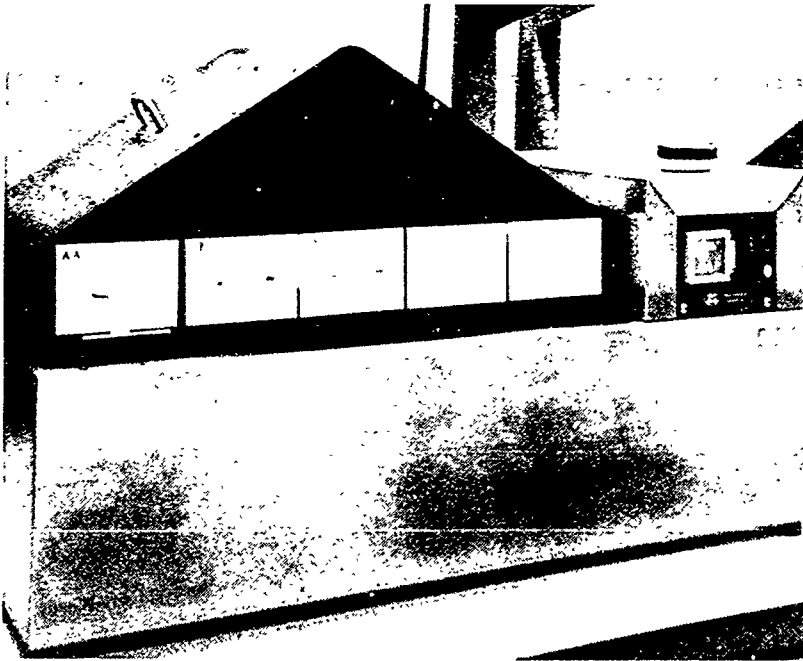
Figure 1 - Mountaingate Steam Ager

Steam Ager Conditions
Weight Gain of Cu Coupons vs Temperature
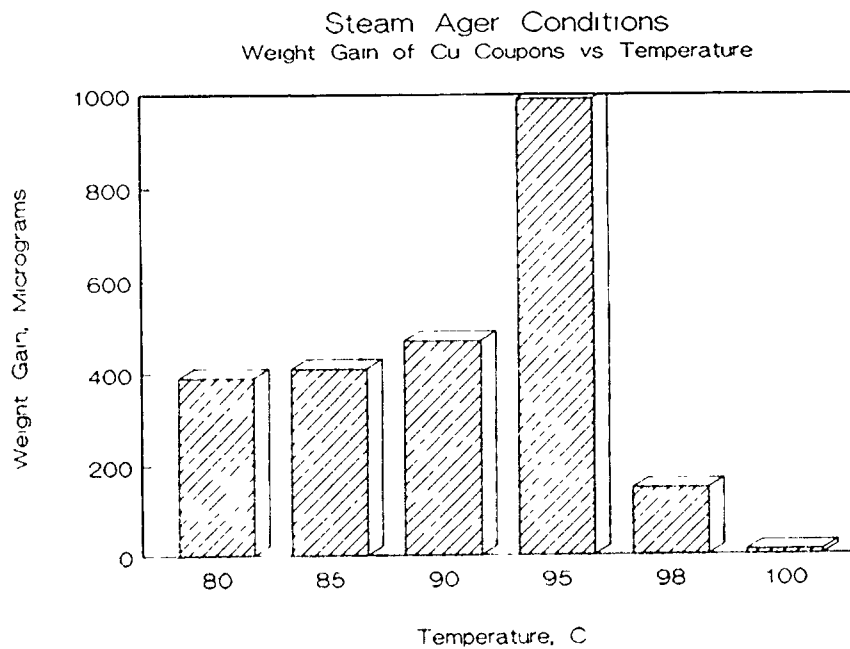
Figure 2 - Average weight gain of copper coupons vs temperature in a Mountaingate Steam Ager.

Steam Ager Conditions
Wt Gain of Sn-Pb Coupons vs Temperature
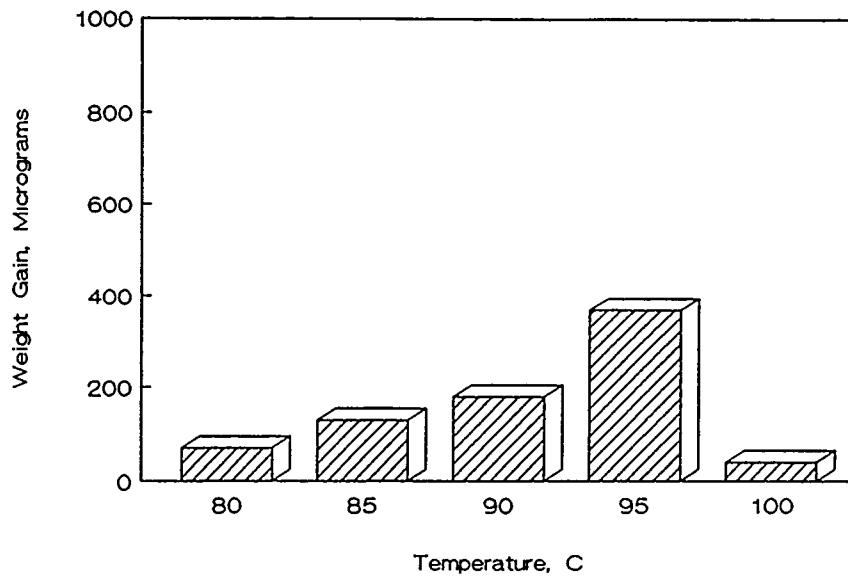
Figure 3 - Average weight gain of 63-37 solder foil coupons in a Mountaingate Steam Ager.

Steam Ager Conditions
Weight Gain of Cu Coupons
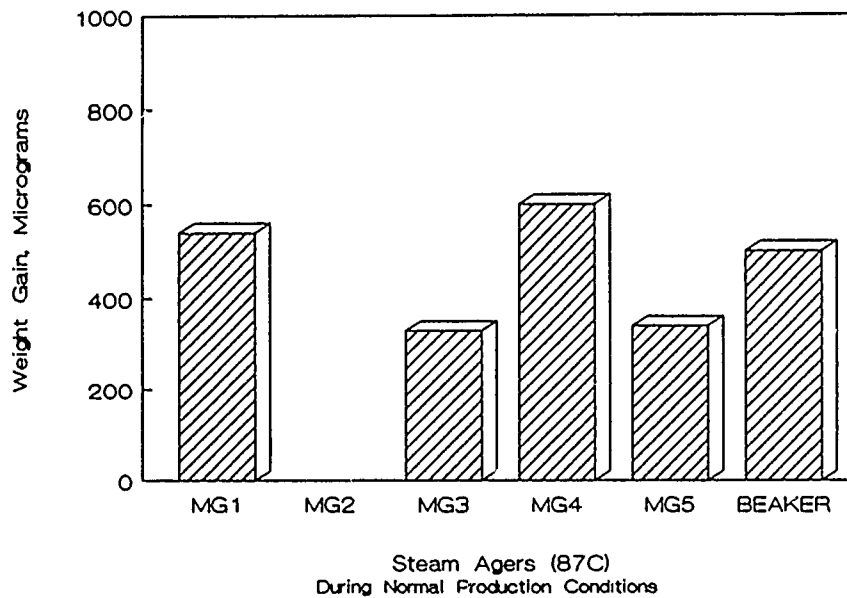
Figure 4 - Average weight gain of copper coupons in various steam agers during normal production conditions (MG = Mountaingate model)

Steam Ager Conditions
Weight Gain of Cu Coupons
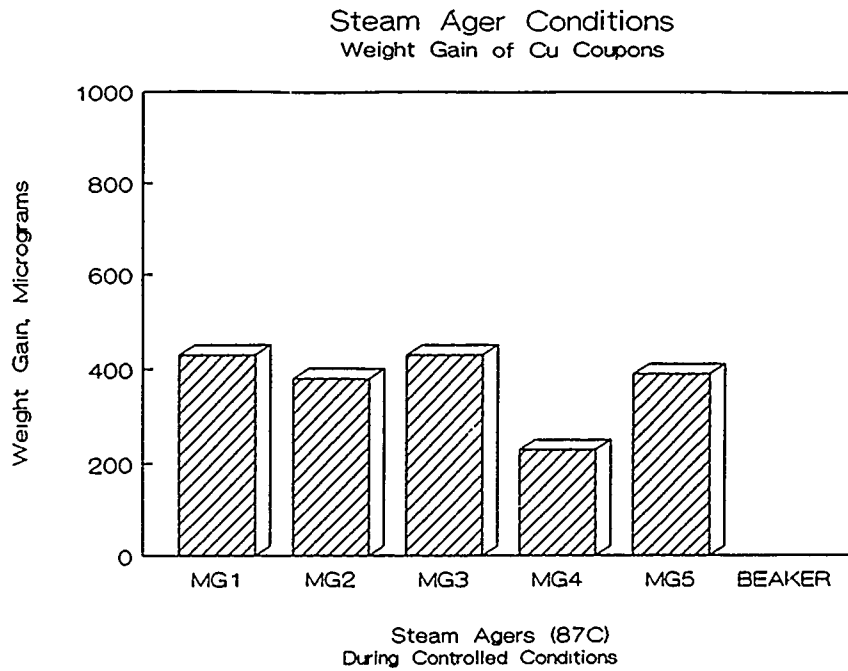
Figure 4A - Average weight gain of copper
coupons during controlled conditions (MG
= Mountaingate Model)

Component Drying Time
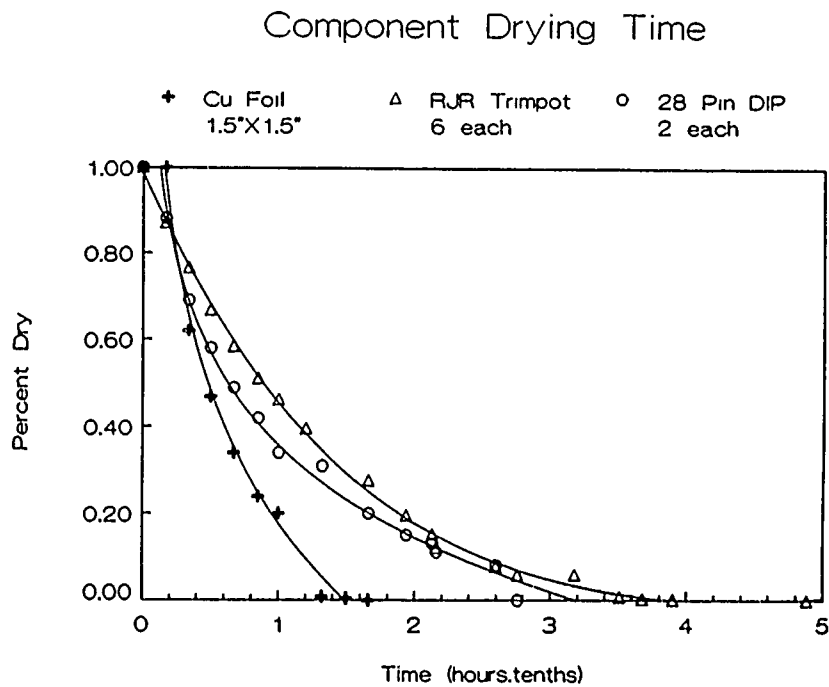
Figure 5 - Required drying time following
steam aging.
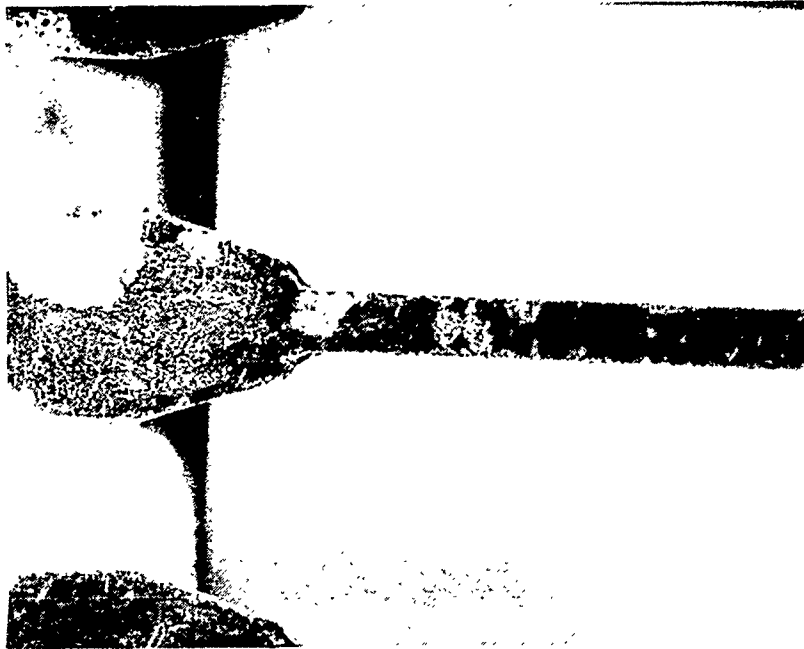
Figure 6 – Photograph of the false dewets
on a part that was dipped too deeply in
the flux during the solder test.

Solderability Inspection Correlation
Process Capability Chart
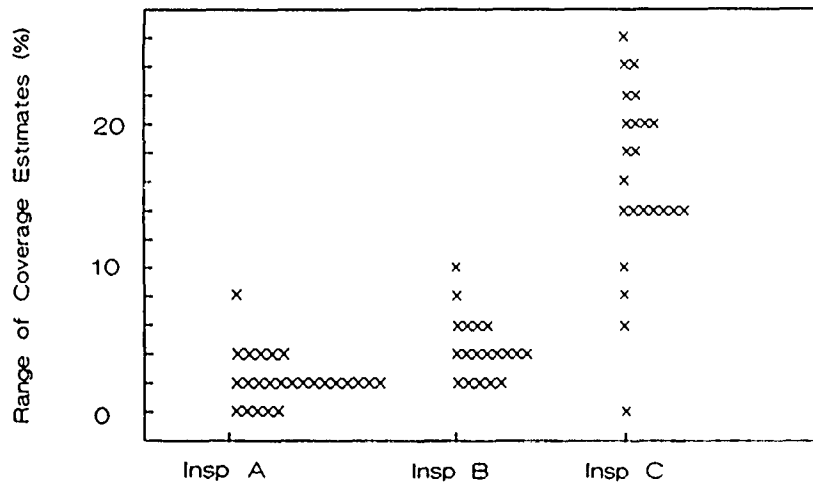
Figure 7 – Histogram showing the
variability of inspector estimates of
solder coverage. Each X represents the
difference between the highest and lowest
of four estimates of solder coverage on a
particular lead.

Table 1 - Oxygen level in a steam ager at 100 percent humidity

Temperature	Vapor Pressure[1] Water (mm Hg)	Vapor Pressure Air (mm Hg)	Oxygen Content[2] (%)
80	355.1	404.9	53.5
85	433.6	326.4	42.9
90	525.76	234.24	30.82
95	633.90	126.10	16.59
100	760.00	0.00	0.00

1.   Please see Reference 3.

2.   Percent oxygen in ager when oxygen in dry air at same temperature is normalized to 100%.

Table 2 - Copper coupon weight gain in Steam Ager

Ager	Production Test		Controlled Test	
	Ave	Std. Dev.	Ave	Std. Dev
MG1	540	150	430	160
MG2	---	---	380	70
MG3	330	120	430	60
MG4	600	100	230	40
MG5	340	110	390	90
Beaker	550	150	----	----

Units: Micrograms

Table 3 – Effects of DI vs Distilled water on
Solderability test results

Part Type	Lots Tested	DI Water		Distilled Water	
		Pass	Fail	Pass	Fail
Connectors	11	9	2	9	2
Discrete SC	8	7	1	5	3
Microcircuits	51	50	1	50	1
Resistors	2	2	0	2	0
Total	72	68	4	66	6

Table 4 – Solderability test results after
alcohol vs air dry

Drying Method	No. Parts	Observations	
		Surface Roughness	Dewet/ Nonwet
120 min in air	25	24	24
10 min in IPA, 10 min in air	25	6	0

Table 5 – Static vs Flow Pot Test Data – (Data is number of parts, except where otherwise stated.)

| Part Type | Finish | Incoming Area | | | | Pretin Area | |
| | | Static Pot | | Flow Pot | | Flow Pot | |
		Pass	Fail	Pass	Fail	Pass	Fail
Connector	Au/Ni	77	13	85	5	90	0
Connector	Au/Cu	62	28	70	20	47	43
IC	Au/Ni	81	9	77	13	90	0
IC	Sn–Pb/A42	11	19	21	9	29	1
Resistor	Sn–Pb/Cu	30	0	30	0	30	0
Resistor	Sn–Pb/Ni	30	0	30	0	30	0
Totals		291	69	313	47	316	44
Percent		80	20	87	13	88	12

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A PROPOSAL FOR A STANDARD SOLDERABILITY-TESTING METHOD FOR SMD's

by

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1 INTRODUCTION

Generally, the longer it takes for an error to be found, the more expensive it will be to correct. The fastest way to reveal an error in electronic components, is to test them on arrival. This is true both when considering electrical properties as well as solderability.

To be able to test the solderability in a way that both manufacturers and users will accept, there has to be a standardized testing method. This method must be built upon well defined as well as scientifically well founded limits for what is good or bad solderability.

For through-hole mount components there are two objective testing methods standardized by IEC (International Electrotechnical Commission). These are the Solder Globule method and the Wetting Balance method (Reference 1 & 2).

When it comes to surface mounted devices, SMDs, there is no objective method for how to determine solderability. The most widespread and widely used method is the "dip-and-look test", which by no means can be called an objective testing method.

Several people in different places are involved in the work on how to standardize an objective solderability testing method for SMDs. It seems that the most promising way to do this is by using the Wetting Balance, either equipped with a solder bath or with a solder globule ("Micro-wetting method").

2 PROPOSAL FOR A SOLDERABILITY TESTING METHOD

2.1 Introduction

In our solderability tests we utilized a high resolution wetting balance, designed specially to meet our requirements. It is computerized and it is therefore possible to control all the test-parameters directly from an IBM-compatible PC. A schematic picture of the wetting balance, is shown in figure 1.

The solderability tests, which this paper is based upon, have been performed during 1988. Over 500 components, mainly chip-capacitors, have been tested with a wetting balance equipped with a solder bath.

The capacitors were from three different manufacturers of different sizes and with three different types of metallisations on their terminations.

In all tests the wetting force has been registered throughout the whole test, but in many cases the wetting force after two seconds and after ten seconds were explicitly identified (Figure 2). The choice of wetting force reached after two seconds, was based on the testing of through-hole mount components where this is the time within which a certain wetting force must be reached. One reason for measuring the wetting force after ten seconds was that the wetting force then has stabilized on an even level. Another reason is that when an activated flux is used, a peak or "hump" is found on the wetting curve just where the meniscus reaches its maximum height. In some tests this occurs around two seconds so that if the wetting force is then measured after two seconds the value will be invalid. The effect can be seen in figure 4 where the wetting force for the Ni/Sn-capacitor is higher at two seconds than it is at ten seconds.

2.2 Test conditions

Usually, the tests were performed under the following conditions:

	– solder bath.
composition of the solder	– Sn/Pb 63/37.
type of flux	– RMA-flux, according to IEC 68-2-20.
temperature	– 235°C.
immersion speed	– 0.1 mm/s.
immersion depth	– 0.006 mm.
immersion time	– 10 s.
withdrawal speed	– 1 mm/s.
orientation of component	– "standing"

2.3 Tests and results

Our tests show that it works very well indeed to use a wetting balance with a solder bath for SMD-testing. There are some advantages in using a solder bath instead of using a solder globule. The main one is that there are no major problems with heat-transfer when dipping in a bath.

The composition of the solder, immersion time and withdrawal speed were found to have no significant influence on either the wetting force or the wetting time and will therefore not be discussed here. The immersion speed has only an indirect influence on wetting force and time through its effect on immersion depth; the slower the immersion speed, the shallower can be the immersion depth. The most influential factors governing wetting force and wetting speed are the temperature, the immersion depth and the flux.

2.3.1 Flux

The fluxes used in our tests have been a non-activated, R-flux, and a mildly activated, RMA-flux, standardized according to IEC 68-2-20.

The wetting force was lower when the R-flux was used compared to RMA. A lower wetting force and longer wetting time were also found for the R-flux (Figure 3,4 & 5). The spread in the results were also greater for the R-flux than for the RMA-flux (Figure 6).

Most users tend to use a flux with the necessary degree of activation, although there are a small number of users who must use a non-activated flux. Some arguments have been raised for only using a non-activated flux for solderability testing. One reason is that non-activated flux is said to be the only type of flux where the constituent elements are known. This comment is no longer a valid argument because a mildly activated flux is standardized by IEC where its contents are strictly defined.

Our proposal is open for both a non-activated and a mildly activated flux as long as they follow the standard in IEC 68-2-20. A user who uses a non-activated flux in his production has nothing to gain in using a mildly activated flux in his solderability tests. There are some practical advantages in using a mildly activated flux, such as the higher wetting force which this produces and the associated ease of measurement.

2.3.2 Temperature

The temperature dependence of both wetting force and wetting time was tested. The wetting force was measured after two and after ten seconds at four different temperatures. These were 190°C, 210°C, 235°C and 260°C. The components used were from the same manufacturer, of the same size (1210) and with the same kind of metallisation (Ni/Sn).

The wetting time, defined as the time it took to reach a normalized wetting force of 50 mN/m, decreased with increasing temperature. Above 230°C the wetting time was more or less constant. The spread in the results was greater at lower temperatures than at higher (Figure 7).

The studies on wetting time also showed that out of 38 tested capacitors 31 reached 50 mN/m within 1.5 s. Of the remaining 7 which took longer time than 1.5 s, 6 were tested at 190°C and one at 210°C (Figure 8).

The wetting force, measured after 2 s, increased with increasing temperature. When the wetting force was measured after 10 s it was nearly constant at all the different temperatures (Figure 9).

It seems that when the component finally reaches the solderable temperature, the meniscus will rise to more or less the same height on all the tested components and, therefore, all of them, independent of temperature, gain almost the same wetting force.

With a lower solder temperature it will take a longer time for the component to reach a solderable temperature, i.e. the lower the temperature, the longer the wetting time.

The most common technique for soldering through-hole mount components is wave-soldering with temperatures for the molten solder around 250°C. To be sure to find the components with good solderability and reveal the ones with bad, the temperature when testing through-hole mount components was set to 235°C. This temperature is proposed as a test temperature for SMDs as well. However, for SMDs it is very common to use reflow soldering techniques, IR and vapour phase, and the working temperature in these techniques are below 235°C. The real temperatures in the solder joints during soldering are often not more than 200°C (Reference 3). If one is to use the same argument for SMDs as was done for through-hole mount components, *the test temperature ought to be well below 235°C, maybe 210°C.*

2.3.3 Immersion depth and immersion speed

Three different types of component were used for the test on how the immersion depth influences the wetting force and the wetting time. These components were: a chip-resistor, 1206, Ni/Sn; a large chip-capacitor, 1812, Ag/Pd and a small chip-capacitor, 0603, Ni/Sn. Ten components of each type were tested.

With an immersion depth of 0.10 mm there was a reduction in wetting force registered for all of the components compared to the wetting force registered when the immersion depth was 0.00 mm. To be able to make a direct comparison between the three types of components with differently sized metallisations, the wetting forces were divided by the wettable perimeter. This is hereby called the normalized wetting force and discussed more thoroughly in paragraph 3.1. The decrease in normalized wetting force were 32% for the chip-resistor, 27% for the small chip-capacitor and 21% for the large chip-capacitor (Figure 10).

The vertical extension of the land on SMD-chips is seldom more than 0.5 mm and often less. The meniscus will, if free to do so, rise to around 3 mm. Therefore it is the extension of the land which provides the limiting factor for the meniscus to rise. When immersed into the solder bath the land will be vertically more shortened and the meniscus height even more limited (Figure 11). As the wetting force is dependent on the meniscus rise, there will always be a decrease in wetting force with increasing immersion depth.

For the small chip-capacitor (0603) an immersion depth of 0.10 mm. will take a greater percentage of the land than it will for the large chip-capacitor (1812). The decrease in wetting force will be accordingly larger for the smaller capacitor than for the larger one.

The conclusion of these tests is that the immersion depth must be very shallow in order to get as high a wetting force as possible. *Our recommendation is, that an immersion depth of 0.01 mm is to be used.*

The immersion speed has only an indirect effect on the wetting force and the wetting time, i.e. the higher the immersion speed, the greater the immersion depth. *We see no reason to propose a certain immersion speed*; the only important thing is that the immersion speed is *sufficiently low to guarantee an accurate immersion depth of 0.01 mm.* The immersion speed will therefore be individual for each type of wetting balance.

3 THE INFLUENCE OF METALLISATION AND COMPONENT SIZE.

3.1 Introduction

The metallisation of the chip-capacitors we tested were of three different kinds. One type had ordinary silver-palladium paste burnt in on its terminations, hereafter this type will ᴜe called Ag/Pd. Another one had additional element or elements in the silver-palladium paste to increase the solderability. This one will be referred to as E/Ag/Pd. The last one that we have tested has silver on the terminations and upon the silver there is an electrolytically plated nickel-barrier. On top of the nickel-barrier there is a tin-layer, either pure tin or with some lead in it, to protect the nickel-surface. We will call this type Ni/Sn.

The influence of size, i.e. the wettable perimeter, of the component and the type of metallisation has been studied in relation to wetting force and wetting time. A study of the relationship betveen normalized wetting force and wettable perimeter was carried out. This concerned six "groups" of capacitors from one manufacturer and with the same type of metallisation, Ni/Sn. Another study to see how the metallisation on the terminations affected the wetting force, the wetting time and the wetting speed was also done. Capacitors from another manufacturer and with three different types of metallisation; Ag/Pd, E/Ag/Pd and Ni/Sn, on the terminations were used.

3.2 Normalized wetting force

To be able to compare the wetting forces from differently sized components we needed to standardize the wetting force in some way. Reference 4 did this for through-hole mount components by dividing the wetting force by the wettable perimeter. For SMDs two possibilities were tried; how the wetting force correlated with the metallised area of the land as well as with the wettable perimeter of the component.

The wetting forces after 2 s and after 10 s were identified. There are straight line relationships between the wetting force and the metallised area of the land as well as between the wetting force and the wettable perimeter (Figure 12a,b). We choose to use the wetting force divided by the wettable perimeter as a normalized wetting force. The reason for this is simply that it is much easier to measure the wettable perimeter than the metallised area.

The normalized wetting force for all the tested capacitors were divided into classes and the number in each class were plotted against normalized wetting force. The distribution was found to be approximately gaussian (Figure 13). The reason for this procedure was to see how the different size-classes and the different metallisations were distributed in the curve with all the capacitors.

3.3 Metallisation

The distribution of the three different metallisations compared to the distribution of all the capacitors as a whole is shown in figure 14. The lowest value of normalized wetting force was found for the smallest of all the tested capacitors, size 0603 and with Ni/Sn-metallisation. Also the largest capacitor, size 1812 with Ag/Pd-metallisation, had low normalized wetting force values. Otherwise, the normalized wetting forces for the different metallisations were evenly distributed (Figure 14). The different size-classes were also distributed evenly.

When the three types of capacitors with the size 1206 were compared with each other and the wettable perimeter was measured, it was found that Ag/Pd and E/Ag/Pd has a wettable perimeter of 4.4 mm whilst Ni/Sn had only 4 mm. The Ni/Sn-capacitor was in other words slightly smaller. This is probably the explanation as to why the final wetting force, i.e. the wetting force after 10 s, was higher for Ag/Pd and E/Ag/Pd than for Ni/Sn (Figure 4).

The wetting time was much shorter for Ni/Sn than it was for Ag/Pd and E/Ag/Pd (Figure 5). This can also clearly be seen in figure 3, where a R-flux was used and the wetting force was measured after 2 s. The wetting force was much higher for Ni/Sn than it was for Ag/Pd and E/Ag/Pd. In fact, Ni/Sn almost reached its final wetting force after 2 s, while the wetting forces for Ag/Pd and E/Ag/Pd was much higher when measured after 10 s than it was after two seconds. In other words, the wetting speed is much higher for Ni/Sn than it is for Ag/Pd or E/Ag/Pd, but the final wetting force is not necessarily higher.

3.4 Size

The size of the component had no significant influence on normalized wetting force, but the wetting time increased with increasing wettable perimeter (Figure 15). The reason for the increasing wetting time is probably the fact that larger components take longer time to reach a solderable temperature than do smaller ones because of their larger mass.

3.5 Discussion, size and metallisation

For the smallest capacitor (0603, Ni/Sn), the normalized wetting force was low. The wetting force is dependent on the meniscus height; the higher the meniscus, the larger the wetting force. The vertical extent

of the land on this capacitor is very small. Therefore, even though the solderability is excellent, the wetting force and consequently the normalized wetting force will be low due to the fact that the meniscus rise is extremely limited.

The wettable perimeter does not seem to have enough influence on the wetting force to explain the comparatively low normalized wetting force for the largest capacitor (1812, Ag/Pd). One possible explanation is that the solderability of Ag/Pd is much worse than it is for Ni/Sn. This is somewhat verified by the fact that the largest capacitor with Ni/Sn-metallisation (1210) has the highest normalized wetting force as well as the highest absolute wetting force. However, the results from the comparison between three capacitors with different types of metallisation contradict this.

When the three capacitors with about the same size but with different metallisations were compared regarding wetting force, it was shown that they all reached approximately the same wetting force, but the times to achieve this were different. This is due to differences in wetting speed and, Ni/Sn having a higher wetting speed than Ag/Pd and E/Ag/Pd. Therefore, Ni/Sn reaches its wetting force maxima prior to the other two.

4 PROPOSAL FOR AN EVALUATION OF THE WETTING CURVE

4.1 Chip-components

4.1.1 Chip-capacitors

Several other chip-capacitors, from different manufacturers and with different types of metallisation, were tested. As mentioned earlier, the normalized wetting forces were divided into classes and the number in each class were plotted against normalized wetting force. This were done for the wetting force measured after 2 s as well as after 10 s. The "10 s"-curve was less scattered than the "2 s"-curve (Figure 16). All the normalized wetting force values for the "2 s"-curve were above 40 mN/m and for the "10 s"-curve all were above 50 mN/m.

All of the above mentioned components were stated by the manufacturers to be fully satisfactory with respect to solderability. We therefore tested 20 components for which the solderability was considered to be bad according to a user. Measured after 10 s, 16 of these components had a normalized wetting force less than 50 mN/m. Only 4 reached 50 mN/m or more.

4.1.2 Chip-resistors

Some chip-resistors were also tested to see if a different geometry of the land had any effect on the normaliz·d wetting force. Chip-resistors differ from chip-capacitors in that there is metallisation along the sides

of the resistor whereas the ends of the capacitor are metallised all the way around. All of the tested resistors reached a normalized wetting force of more than 50 mN/m (Figure 13).

4.1.3 Summary

The results from the tests with the "bad" components together with these from the "good" as well as the results from the resistors gave rise to the concept that a normalized wetting force of 50 mN/m might be a plausible limit for what can be considered as good or bad solderability.

The time taken for the capacitors to reach 50 mN/m were measured. Of the 154 capacitors and resistors all but 8 reached 50 mN/m within 1.5 s (Figure 17). As described in paragraph 2.3.2, of the 38 capacitors tested at different temperatures, 31 reached 50 mN/m within 1.5 s. The ones that did not, were tested at temperatures below 235°C.

4.2 Leaded components

Furthermore, 50 SOT-23s from different manufacturers and with different kind of "tinning" on the leads were tested to see if they fitted into the pattern. The wettable perimeter of the leads were measured and the normalized wetting force calculated. These were divided into classes and the number in each class were plotted against normalized wetting force (Figure 18). The normalized wetting force for the SOT-23s were between 250 and 400 mN/m, much higher than the chip-capacitors and the chip-resistors. These values are similar to values given for through-hole mount components in Reference 4. This was more or less expected since the leads of the SOT-23s are much more similar to those of through-hole mount components than are the terminations of the chip-components.

To see if there should be other limits for go/no go for leaded components, the times taken for the SOT-23s to reach a normalized wetting force of 250 mN/m were measured. Of the 40 SOT-23s, 35 reached 250 mN/m within 1.5 s and 37 reached this force within 2 s (Figure 19).

4.3 Round up

For through-hole mount components IPC (the Institute for Interconnecting and Packaging Electronic Circuits) states in a draft to the standard IPC-S-805A (Reference 5), that 200 mN/m within 2.5 s should be the limit for go/no go. According to the experience from the tests of through-hole mount components and on the basis of our results, it is also possible to recommend a certain normalized wetting force that must be reached within a certain time. The normalized wetting force of 50 mN/m and the wetting time of 1.5 s may have to be revised, due to the fact that these tests have been performed at 235°C instead of the proposed temperature of 210°C. However, it does not seem, as mentioned

earlier, that temperature affects the wetting force to any great extent, although it does have some influence on the wetting time. Even at 210°C, 9 out of the 10 capacitors tested reached 50 mN/m within 1.5 s. Perhaps there should be two different normalized wetting forces, one for chip-components and one for leaded components, each to be reached within a specified time.

5 CONCLUSION

Our results shows that it is possible to test SMDs with a wetting balance equipped with a solder bath, if the immersion depth is shallow enough. We wish to recommend, on the basis of our results, that the following values of the parameters when testing SMDs should be:

	– solder bath or "micro-wetting"
type of solder	– Sn/Pb 63/37
type of flux	– R- or RMA-flux, according to IEC 68-2-20
temperature	– 210°C
immersion depth	– 0.01 mm
immersion speed	– sufficiently low that it guarantees an immersion depth of 0.01 mm
immersion time	– 5 s
withdrawal speed	– not necessary to standardize

The method of evaluation described in the text and shown in figure 20 is, in our opinion, very reliable. To use a method in which a certain normalized wetting force is specified to be reached within a specified time also take in consideration the question of wetting speed. A high wetting speed is important so the component accomplish to be wetted by the molten solder during the soldering process.

The values of a standardized wetting force of 50 mN/m and of a wetting time of 1.5 s, are not rigid values. They can be subject to modification and are therefore to be seen as a contribution to the debate.

REFERENCES

1. IEC Publication 68-2-20, 1979 Part 2: Tests – Test Ta: Soldering.

2. IEC Publication 68-2-54, 1985 Part 2: Tests – Test Ta: Soldering. Solderability testing by the wetting balance method.

3. F. Wester, "Lödförfarandets inverkan på ytmonterade kretsars lödfogar", Examensarbete, 1987-1988, p. 23, Dept. of Phys. Metallurgy, Royal Institute of Technology, Stockholm, Sweden.

4. G. Becker, Paper given at the 6th Annual Soldering Technology Seminar, Naval Weapon Centre, China Lake, Cal. Feb. 18, 1982.

5. IPC-S-805A. 1988. Solderability Tests for Component Leads and Terminations, Original Publication January 1985, Revision a Working Draft September 1988.

WETTING BALANCE   IBM—COMPATIBLE PC
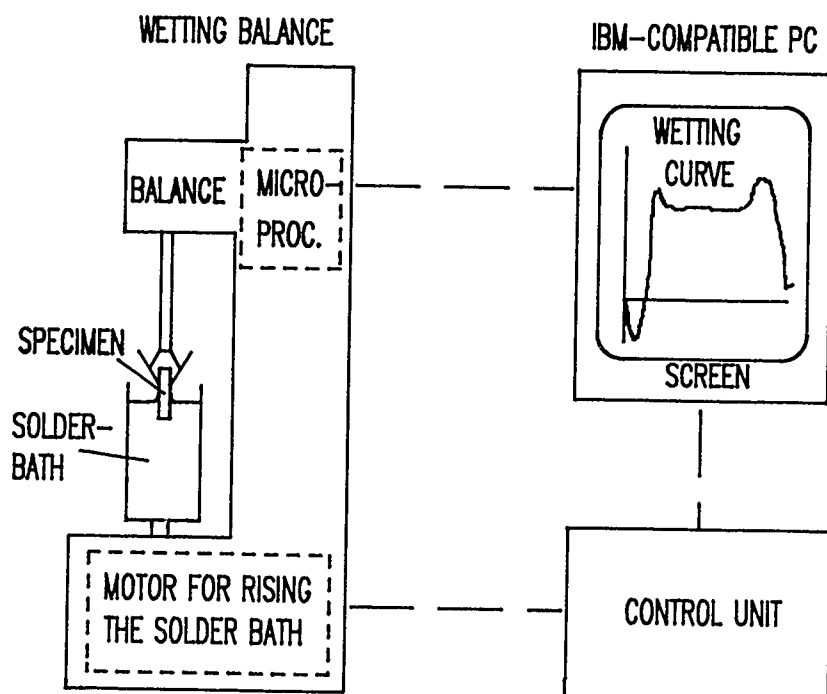
Figure 1. Schematic picture of the wetting balance at the Swedish
Institute for Metals Research. The wetting curve is drawn
on the screen in real time.
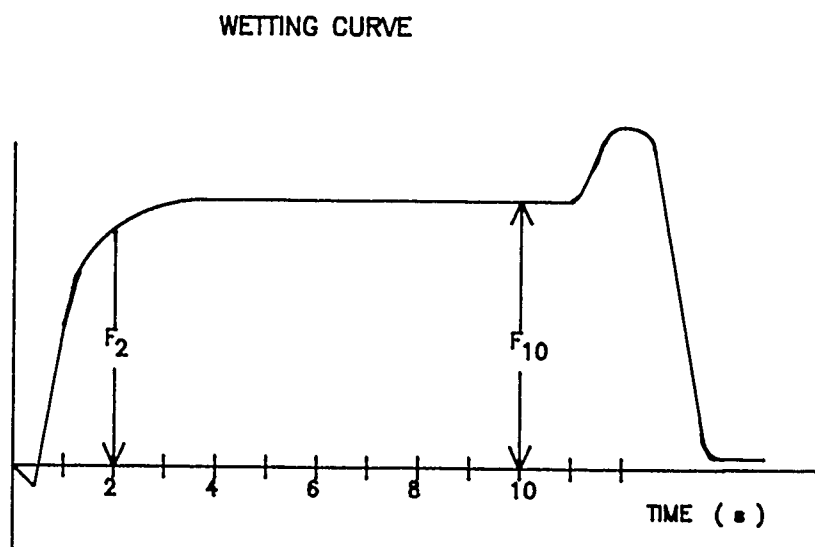
WETTING CURVE

Figure 2. A schematic picture of a wetting curve, i.e. the wetting
force as a function of time. The wetting force is regis-
tered during the whole test, but the wetting forces at
two seconds and ten seconds are explicitly identified.

64
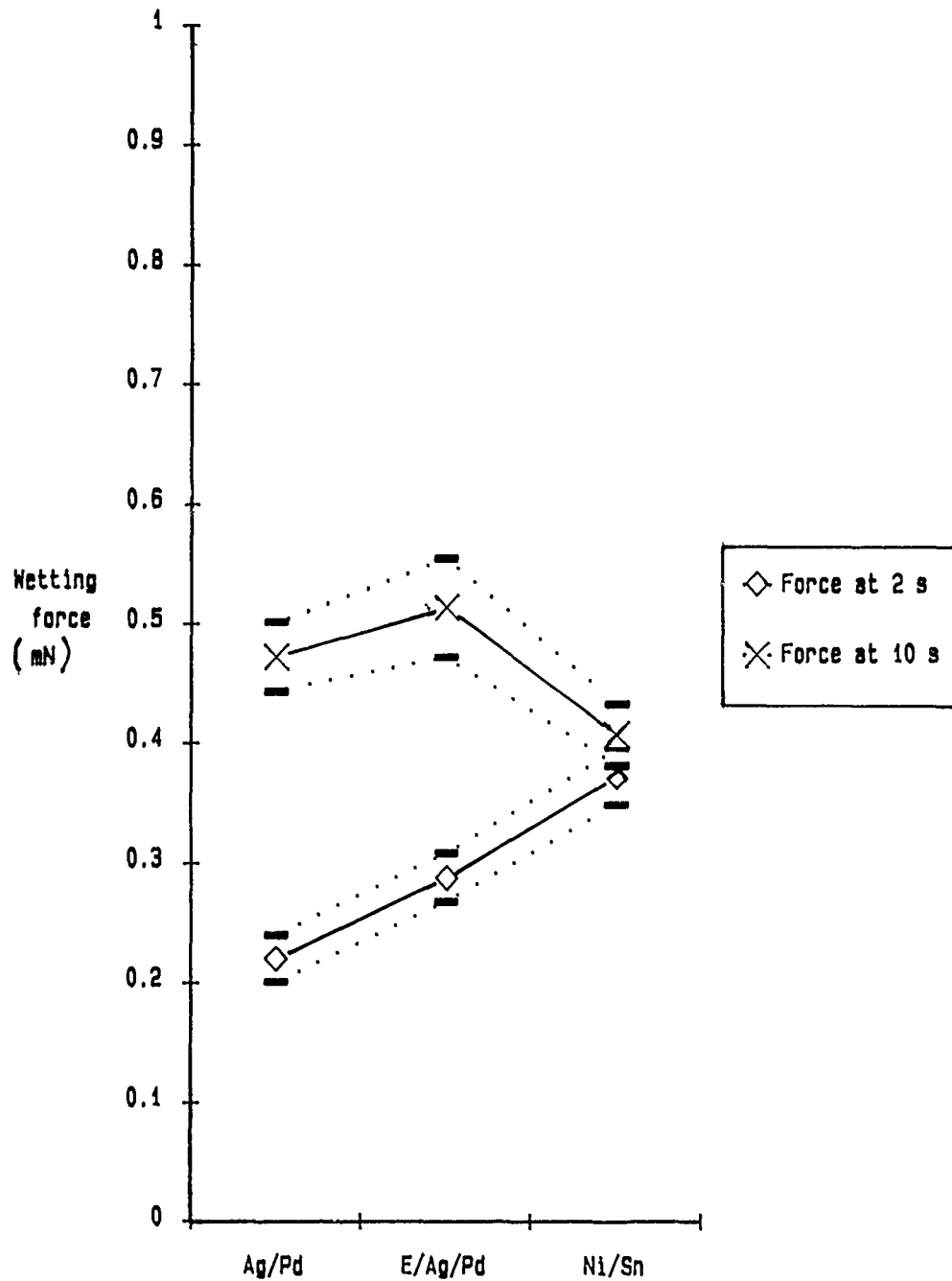
Figure 3. R-flux.
The wetting force measured after two and ten seconds for chip-capacitors with three different types of metallisations.
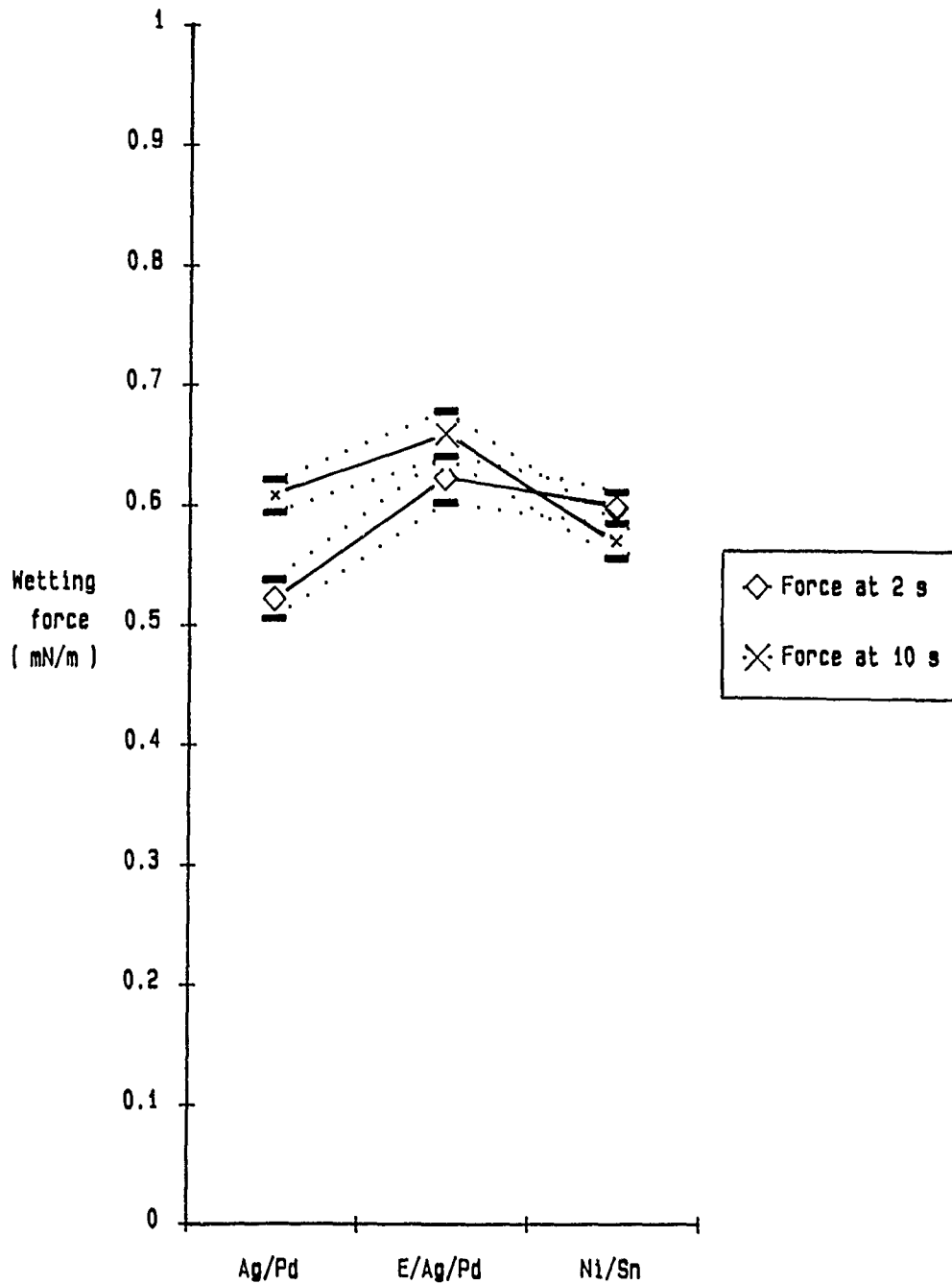
Figure 4.   RMA-flux.
The wetting force measured after two and ten seconds for chip-capacitors with three different types of metallisations.
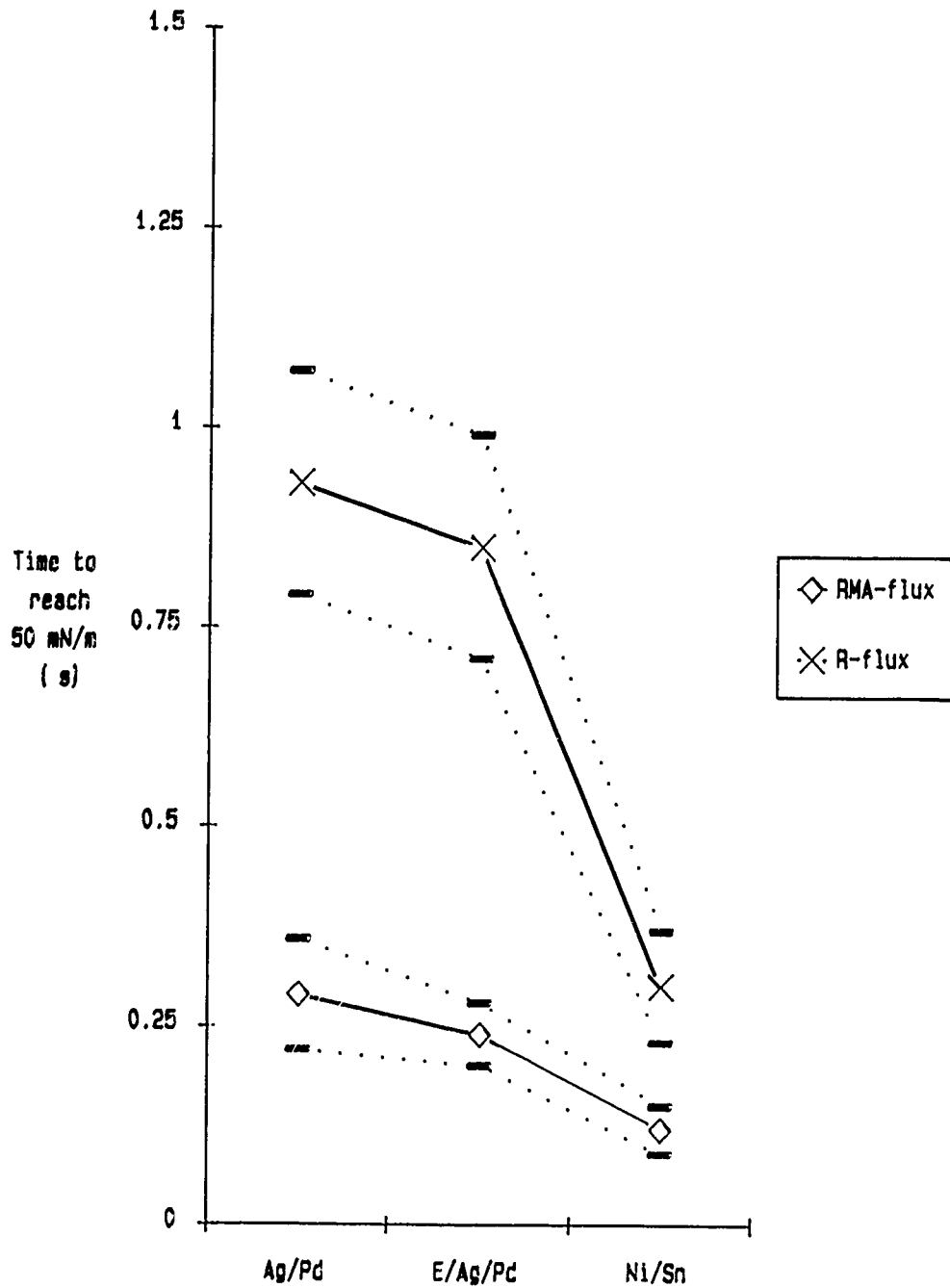
Figure 5. A comparison of the wetting time for three different metallisations and two different fluxes, R-flux and RMA-flux.
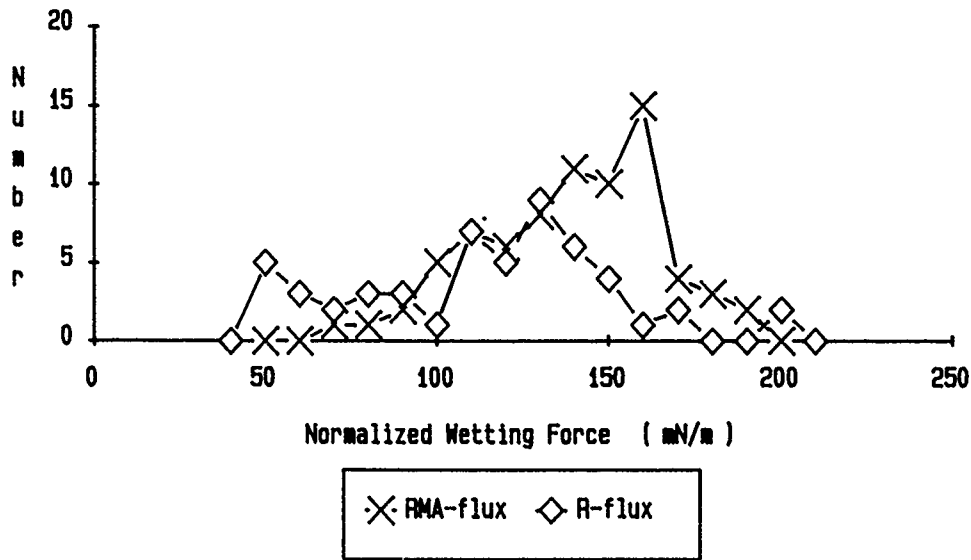
Figure 6. A comparison between normalized wetting force when using R-flux or RMA-flux. The "R"-curve is more scattered than the "RMA"-curve.
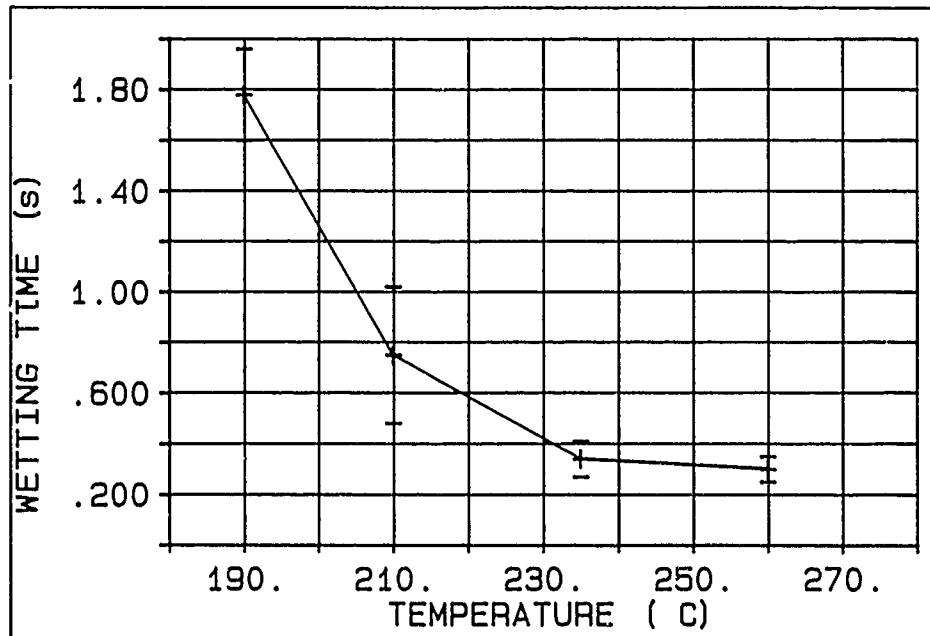
Figure 7. The time to reach the normalized wetting force of 50 mN/m as a function of temperature. The marks (-) over and under the average values (+) indicate the spread in wetting force. Chip-capacitors, Ni/Sn, 1210.
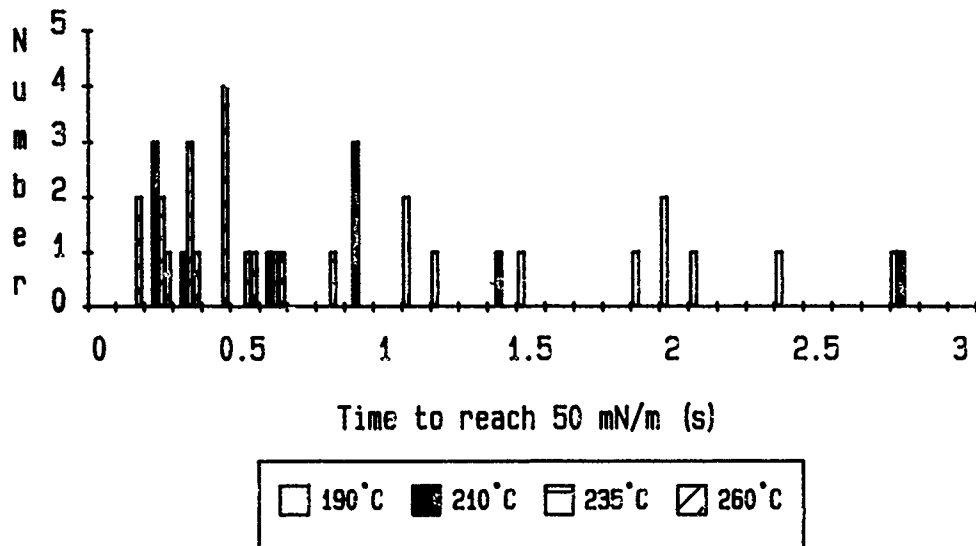
Figure 8. The time to reach the normalized wetting force of 50 mN/m for chip-capacitors (Ni/Sn, 1210) tested at four different temperatures. Of 38 tested capacitors all but 7 managed to reach 50 mN/m within 1.5 s.
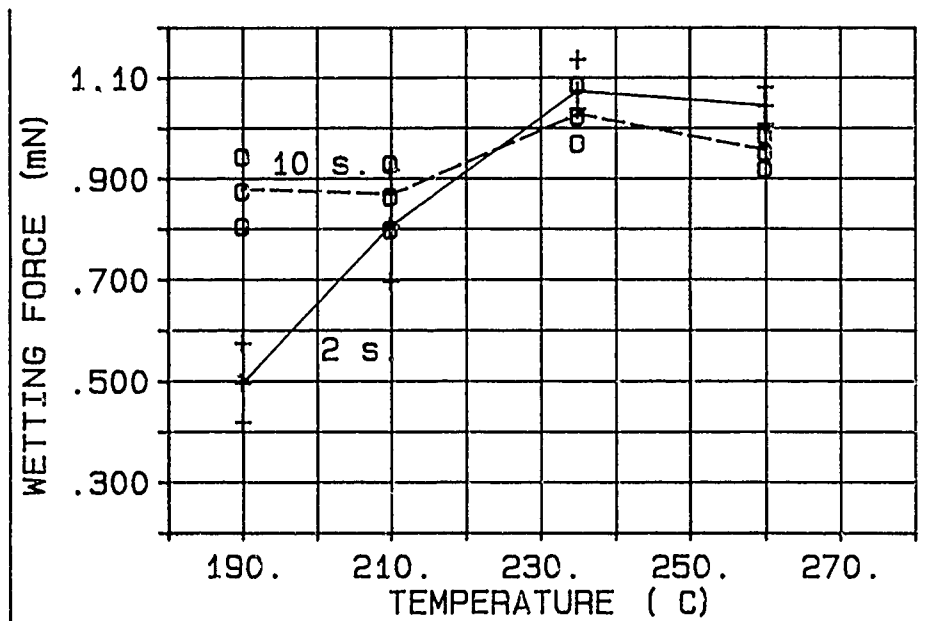
Figure 9. The wetting force as a function of temperature.
+---+--- wetting force measured after two seconds.
o- -o- - wetting force measured after ten seconds.
The marks over and under the lines indicates the spread in the results.
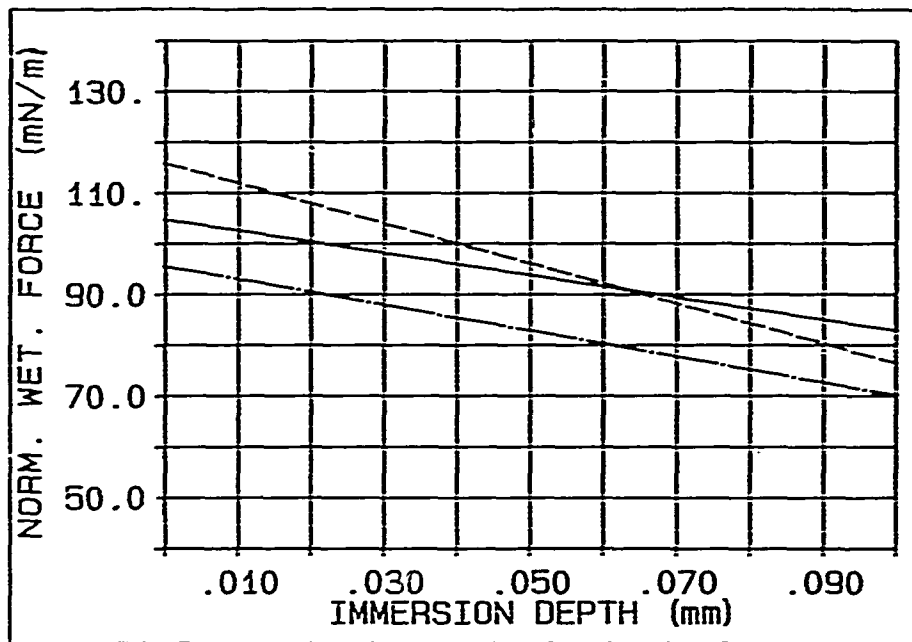
Figure 10. The normalized wetting force as a function of immersion
depth
for three different chip-components.
- - - chip-resistor, Ni/Sn, 1210.
------ chip-capacitor, Ag/Pd, 1812.
-- -- chip-capacitor, Ni/Sn, 0603.
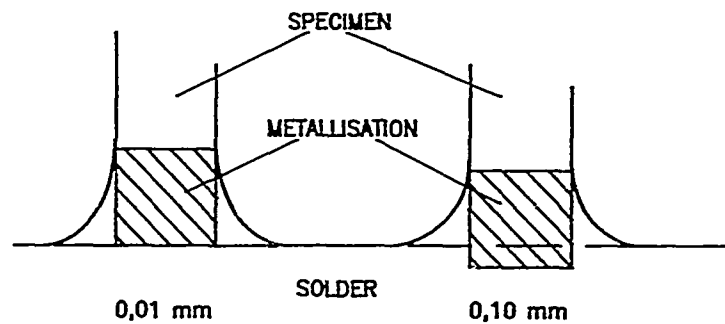
Figure 11. Relationship between the meniscus height and immersion
depth. The land on the chip-component is the limiting
factor for the meniscus possibility to rise. The greater
the immersion depth, the smaller the possibility for the
meniscus to rise.
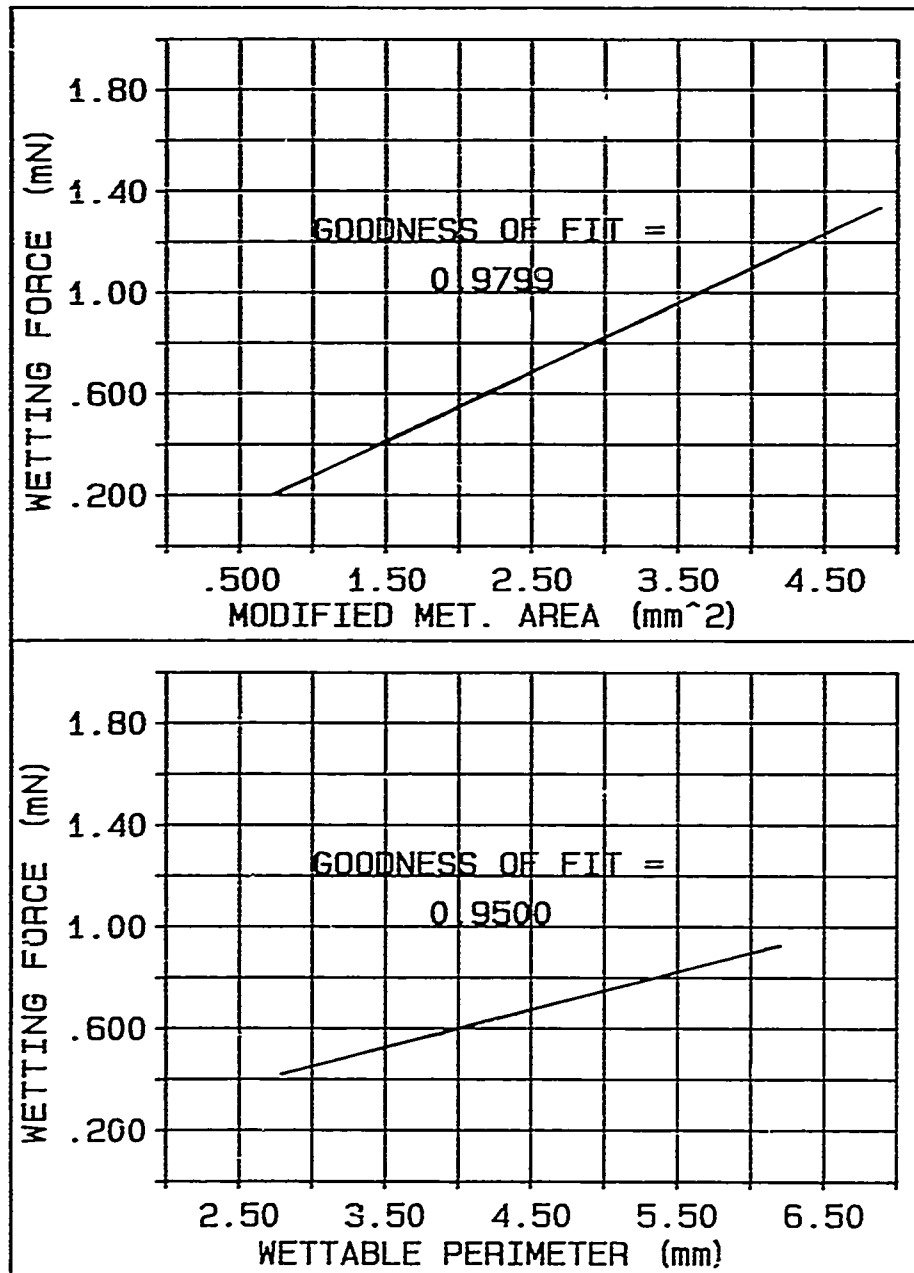
Figure 12. The wetting force as a function of modified metallised
area and as a function of wettable perimeter. Modified
metallised area is the total metallised area minus the
bottom area, this is due to the fact that the metallisation
beneath the solder surf: e during the immersion does not
affect the wetting force.
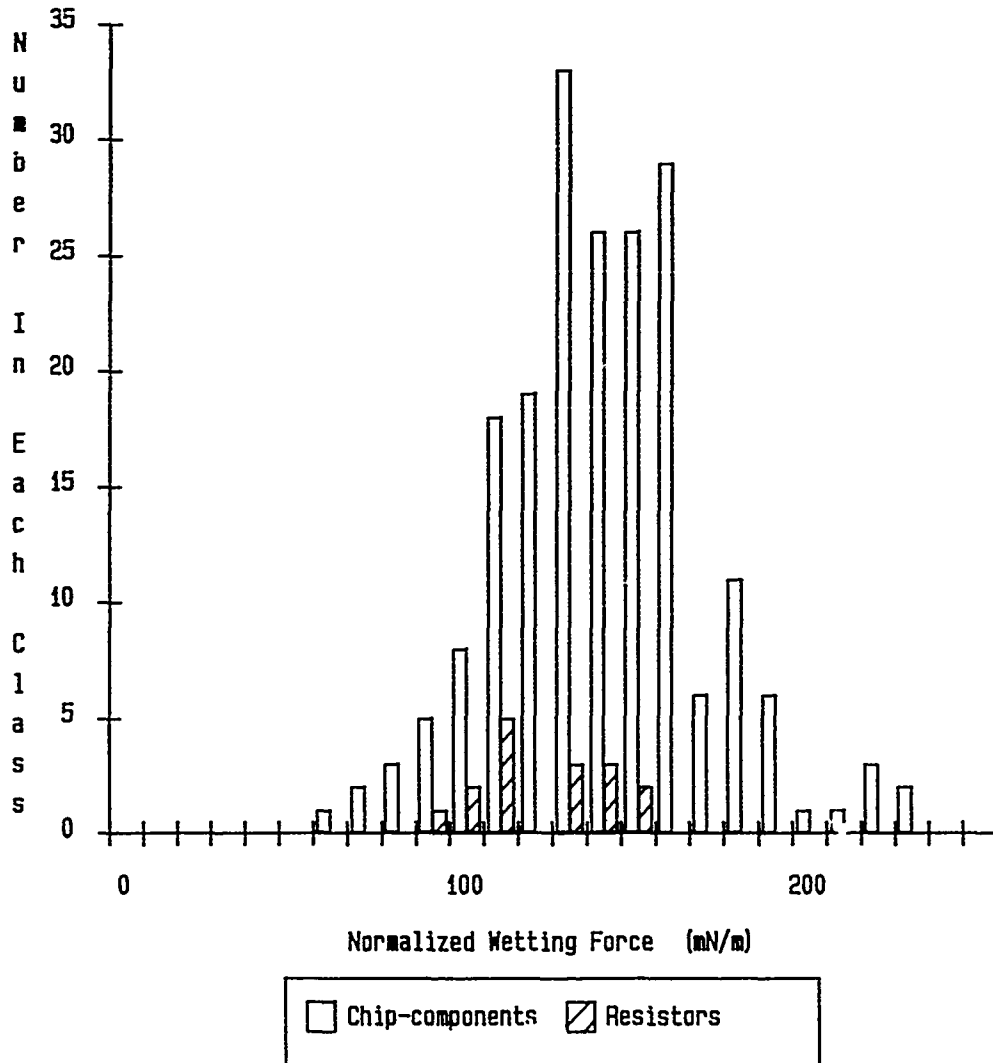
Figure 13. The normalized wetting force for all tested, "good",
chip-components, blank columns. The chip-resistors are
marked with stripes.
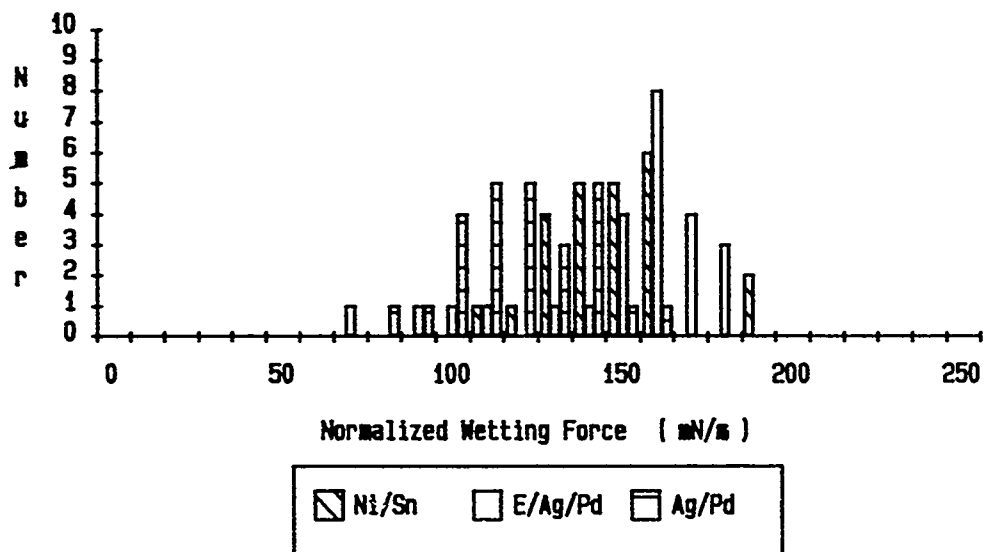
Figure 14. The normalized wetting force for three different types of metallisations.
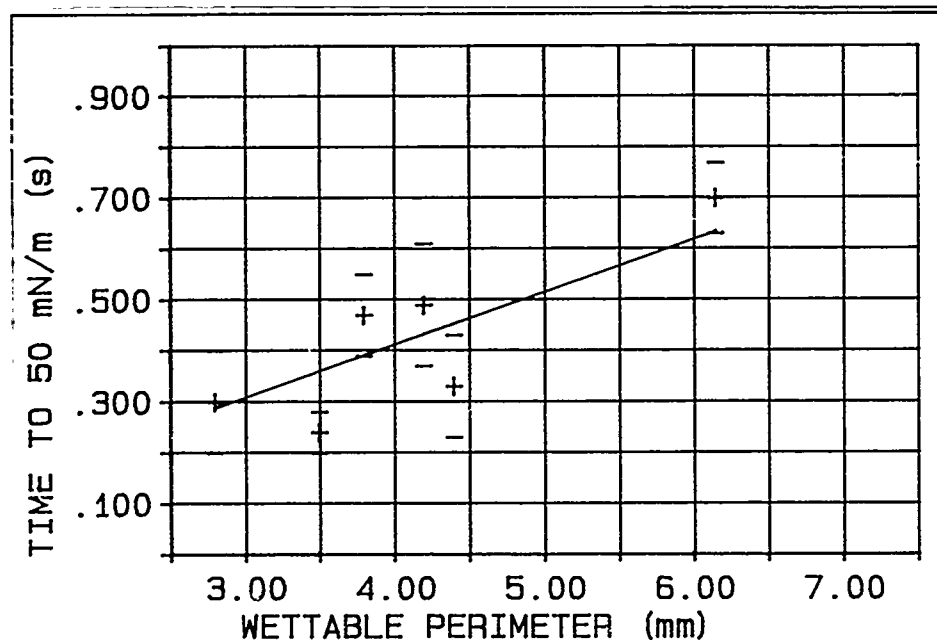
Figure 15. Wetting time against wettable perimeter; the longer the wettable perimeter, the longer the wetting time.
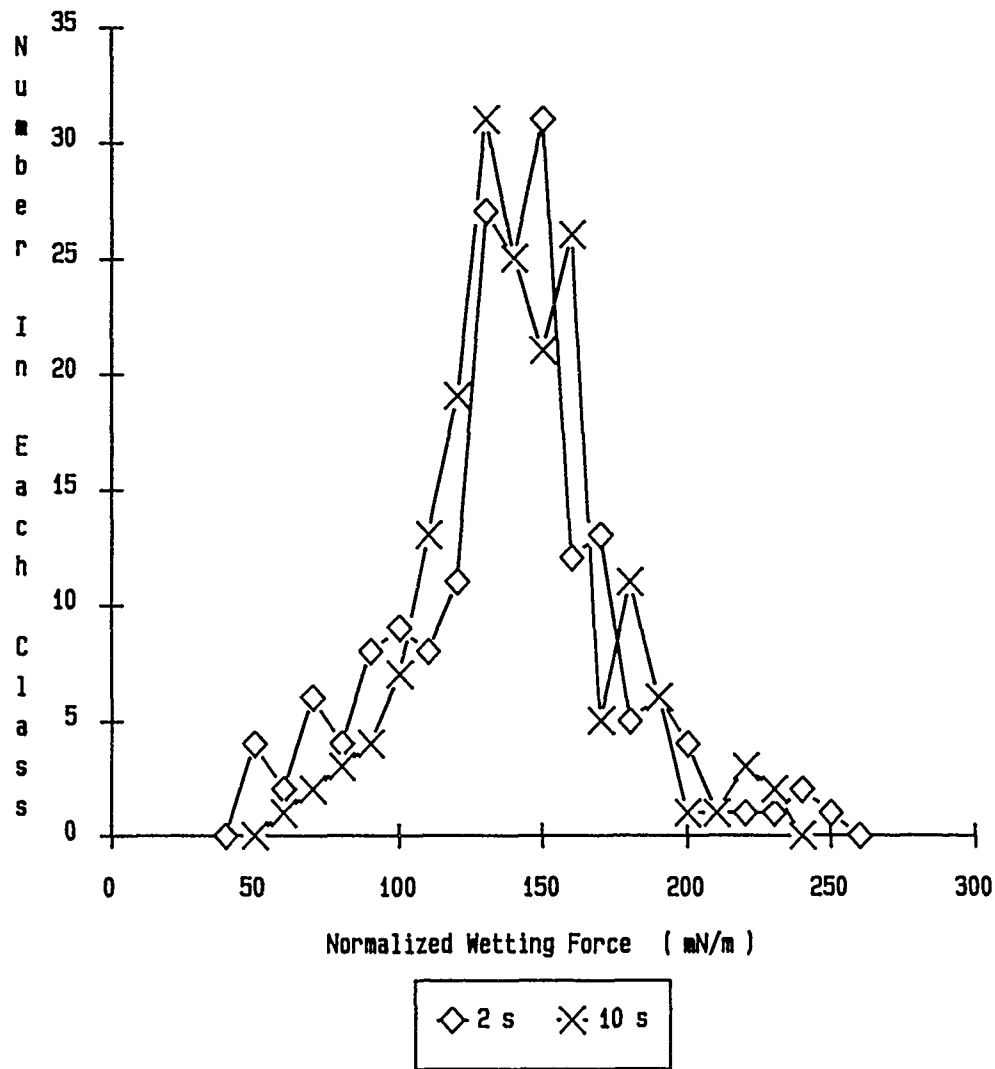
Figure 16. The di. 'erence in normalized wetting force when measured
after two seconds or after ten seconds. The "2 s"-curve
is more scattered than the "10 s"-curve.
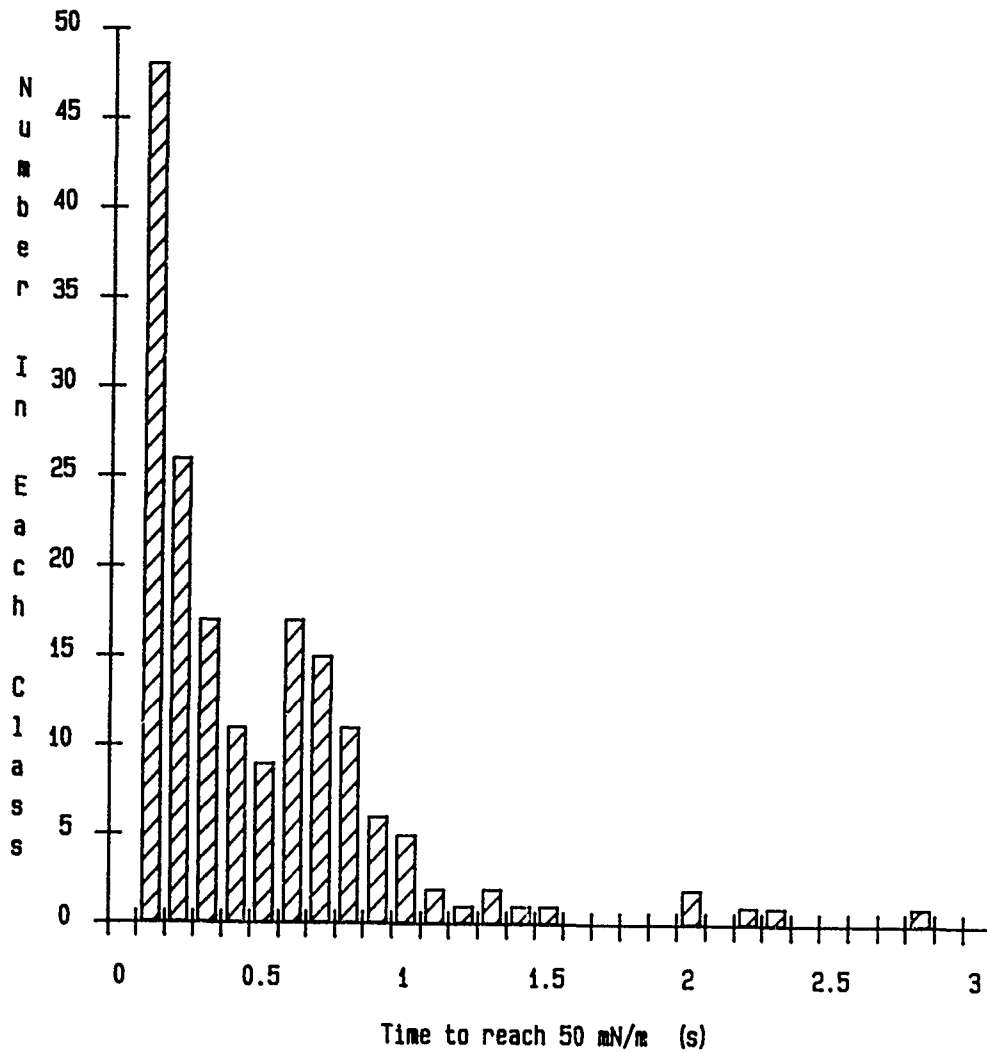
Figure 17. The time to reach the normalized wetting force of 50 mN/m for all the tested, "good", chip-components. Of 154 tested all but 8 reached 50 mN/m within 1.5 s.
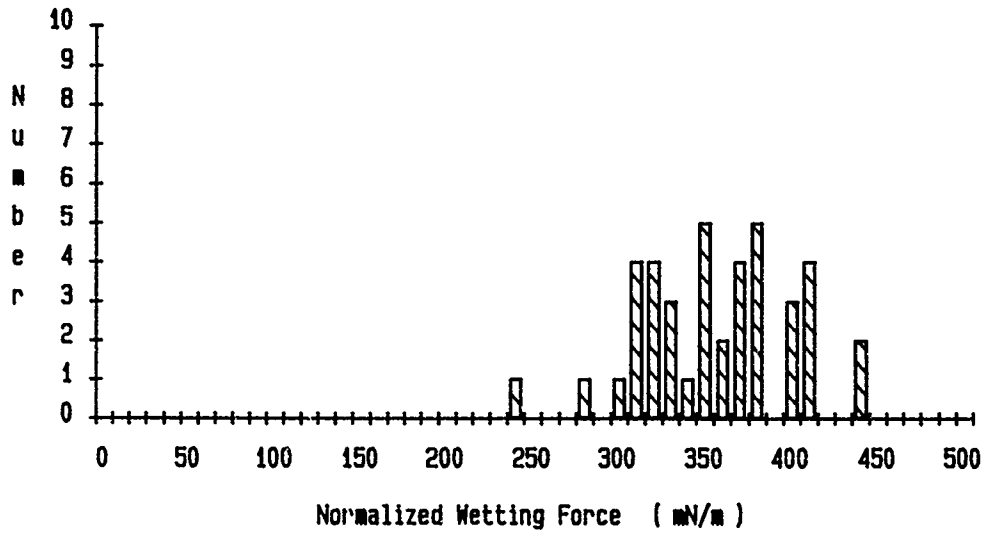
Figure 18. The normalized wetting force for 50 SOT-23s. Compared to the chip-components, the normalized wetting forces for the SOT-23s are much higher.
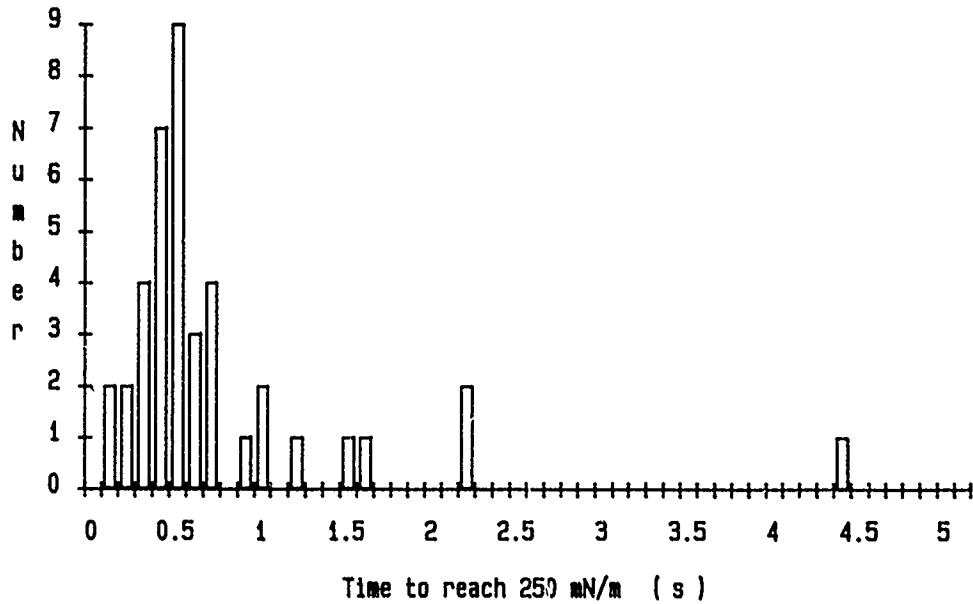
Figure 19. The time taken for SOT-23s to reach the normalized wetting force of 250 mN/m.
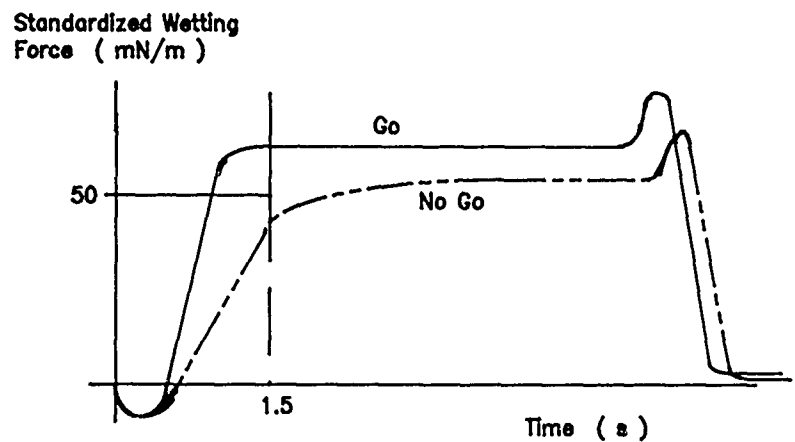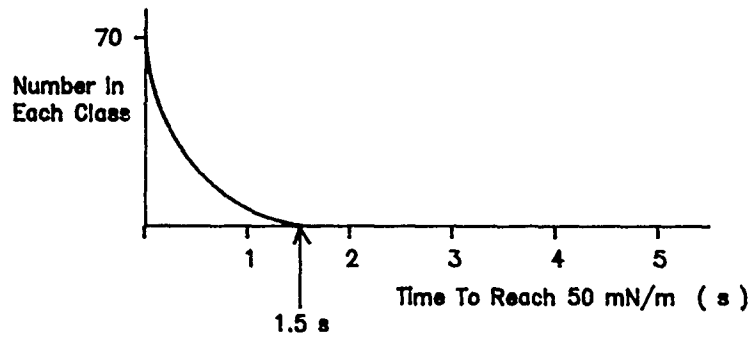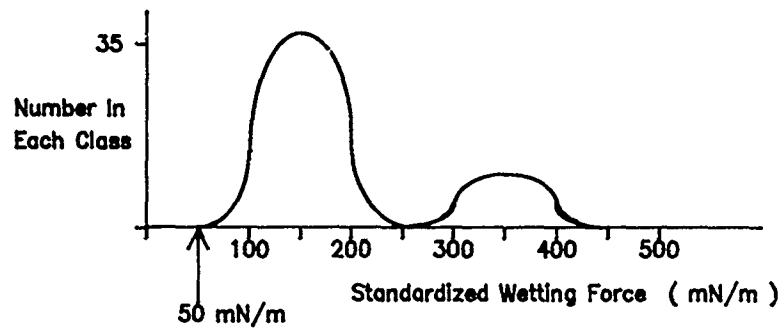
Figure 20. A proposal for how to determine solderability. A certain standardized wetting force, e.g. 50 mN/m, must be reached within a certain time, e.g. 1.5 s.

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WAVE SOLDER PARAMETER OPTIMIZATION USING
A STATISTICAL EXPERIMENTAL DESIGN

by

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ABSTRACT

One part of putting a new wave solder machine into service is determining the optimum settings for the machine's operating parameters. Generally this is done on the basis of "common" knowledge or by simply using whatever settings were used on the old machine.

In this case a full factorial statistical experiment was designed and performed to determine the optimum settings for conveyor speed, board topside temperature, and solder pot temperature. Using this technique it was possible to determine the size and shape of the optimum processing "window" by constructing contour plots from the data. The experiment was repeated for a different assembly to determine the sensitivity of the parameter settings to board thickness and component density.

INTRODUCTION

Statistical experimental design has been in use in this country since at least 1935 (Reference 1). Until recently the technique has found application mostly in the chemical process (Reference 2) and agricultural industries. The technique is useful for designing experiments in which there are multiple independent variables and some degree of interaction between variables. The technique should not be confused with Statistical Process Control (SPC), which deals with controlling a process once the experimental work is done and the process operating parameters have been established.

The classical method for designing an experiment is to pick one variable, change it in small steps, and measure the response of one or more dependent variables. For this method to be valid the following assumptions must be true:

1. The response is a complex function of any single variable. This means that many runs (small increments) will be necessary to characterize the response.
2. There are no interactions between independent variables.
3. The experimental error is small with respect to the change in response due to the selected increment of the independent variable.

The statistical method is based on a different set of assumptions:

1. The response functions are not complex (simple curvature at most). This means that only a few increments of the independent variables will be needed to characterize the response.
2. There are interactions between independent variables.
3. The experimental error is large with respect to the increment of response.

In some cases the classical method will give better results, but in general, the statistical method will give better results at a lower cost. The principal advantages are that experimental error can be measured and eliminated, fewer experimental runs are needed, and interactions between independent variables can be explored.

The essence of this paper is the experimental method, not the results of the experiment. The author's intent is not to define the correct operating parameters for all wave solder machines, but to demonstrate a method for determining the optimum parameters for any wave solder machine in its own unique environment.

For a detailed description of how to do a statistical experimental design, see References 2 and 3. Reference 2 in particular presents a "cookbook" approach to statistical experimental design.

BACKGROUND

The experiments described in this paper were done as part of the installation of a new wave solder machine at the Collins Defense Communications facility in Richardson, Texas. The purpose of the experiments was to test whether the "common" knowledge about the optimum conditions for wave soldering were indeed true. The parameters tested were solder pot temperature, board topside temperature, and conveyor speed. A statistical experimental design was adopted in order to determine the optimum settings of these three parameters, and how large the processing window would be. That is, how far could the settings vary from optimum without a significant increase in defects?

The wave solder machine used in the experiment was an Electrovert Century 2000S. This machine can be run in automatic mode, in which the machine parameters are monitored and controlled by a built-in microprocessor. The process parameters which were studied in the experiment are those which can be varied from board to board with relative ease (solder temperature, topside PWB temperature, and conveyor speed). All other variables (flux type, flux density, solder wave height, conveyor angle) were held constant.

The solder temperature is subject to closed loop control in the conventional manner, by a thermocouple in a dry well immersed in the solder pot. The position of the thermocouple is about two inches from the bottom of the solder pot. Note that this means that the actual temperature of the solder wave contacting the board will be lower than the control temperature. It is not known exactly what the difference is, but other sources have suggested that it may be as much as 10 °C.

The conveyor speed also has a closed loop control. The motor shaft rotational speed is sensed and the motor voltage is adjusted to maintain the preset speed. The conveyor speed in and of itself is not terribly important. What the conveyor speed represents is the amount of time any

individual solder joint on the board is exposed to the molten solder in the wave and how much time the board spends in each stage of preheat. Since it was not possible to separate the effects of these two variables within the context of this experiment, they were lumped together under the term "conveyor speed."

The board topside temperature has a somewhat more complex control system. There are two stages of quartz tube preheaters in the machine. The first-stage preheater is controlled by a numerical setpoint and does not have a closed loop control. The board topside temperature is measured by an infrared sensor after the first stage of preheat. The computer then adjusts the intensity of the second-stage preheater based on the desired final temperature, the conveyor speed, and the temperature reading made after the first stage of preheat. Therefore, the second stage of preheat is subject to closed loop control. This control system partially compensates for the difference in thermal mass of various types of assemblies.

It was assumed that the optimum results would be obtained with values of the three variables somewhere within the following ranges:

Solder pot temperature:	480 - 520 °F
Topside board temperature:	180 - 220 °F
Conveyor speed:	1.9 - 5.7 ft/min

The PWBs used in the experiment were multilayer, made from epoxy/glass, solder masked both sides, and had a variety of through-hole mounted components. There were no surface-mounted components on the PWBs.

TEST DESIGN

A rotatable central composite design was used to determine the effects of the three factors on solder defects. The rotatable central composite is formed from a complete factorial design in three factors at two levels each (eight corners of a cube) plus six star points and several repeat center points. The repeat center points provide an estimate of variability or "noise" in the data.

The advantages of a rotatable central composite design are:

1. All main effects (3), all two factor interactions (6) and the three-factor interaction can be estimated. An interaction exists among two or more factors, if the effect of one factor on a response, depends on the levels of other factors.

2. The data can be used to estimate the coefficients of a quadratic model, so response surfaces can be constructed. A response surface is the geometric representation obtained when a response variable is expressed as a function of one or more quantitative factors.

3. The design is rotatable, meaning the model will estimate responses with equal precision at all points in the factor space equidistant from the center.

In the design and analysis of experiments, it is often convenient to express factor levels in coded or standardized form. The factorial points are at the corners of a cube with sides 2 units in length, while the star points are located along each axis a relative distance of 1.68 units from the center of the cube.

Table 1 lists the design points for a rotatable central composite design using coded factor levels.

TABLE 1. Design Points for Rotatable Central Composite Design.

Run No	Factor A	Factor B	Factor C
1	−1	−1	−1
2	−1	−1	1
3	−1	1	−1 Factorial
4	−1	1	1 Points
5	1	−1	−1
6	1	−1	1
7	1	1	−1
8	1	1	1
9	−1.68	0	0
10	1.68	0	0 Star
11	0	−1.68	0 Points
12	0	1.68	0
13	0	0	−1.68
14	0	0	1.68
15-17	0	0	0 Repeats

The actual factor levels used in the experiment correspond to the coded levels as follows:

Coded Level	−1.68	−1	−0.67	0	1	1.68
Solder Pot Temp (°F)	480	488	NA	500	512	520
Board Temp (°F)	180	188	NA	200	212	220
Conveyor Speed (ft/min)	5.7	4.0	3.5	2.8	2.2	1.9

This is shown pictorially in Figure 1. The circles represent the combination of factor levels that constitute an experimental run. Due to a calculation error, the speed corresponding to coded level −0.67 instead of −1 was run in Experiment #1. This did not reduce the amount of information that can be gained from this experimental design.

The experiment was run twice, once with 17 scrap boards (Part No. 656-4045-001) and once with 21 production boards (Part No. 643-6128-002).

ROTATABLE CENTRAL COMPOSITE DESIGN
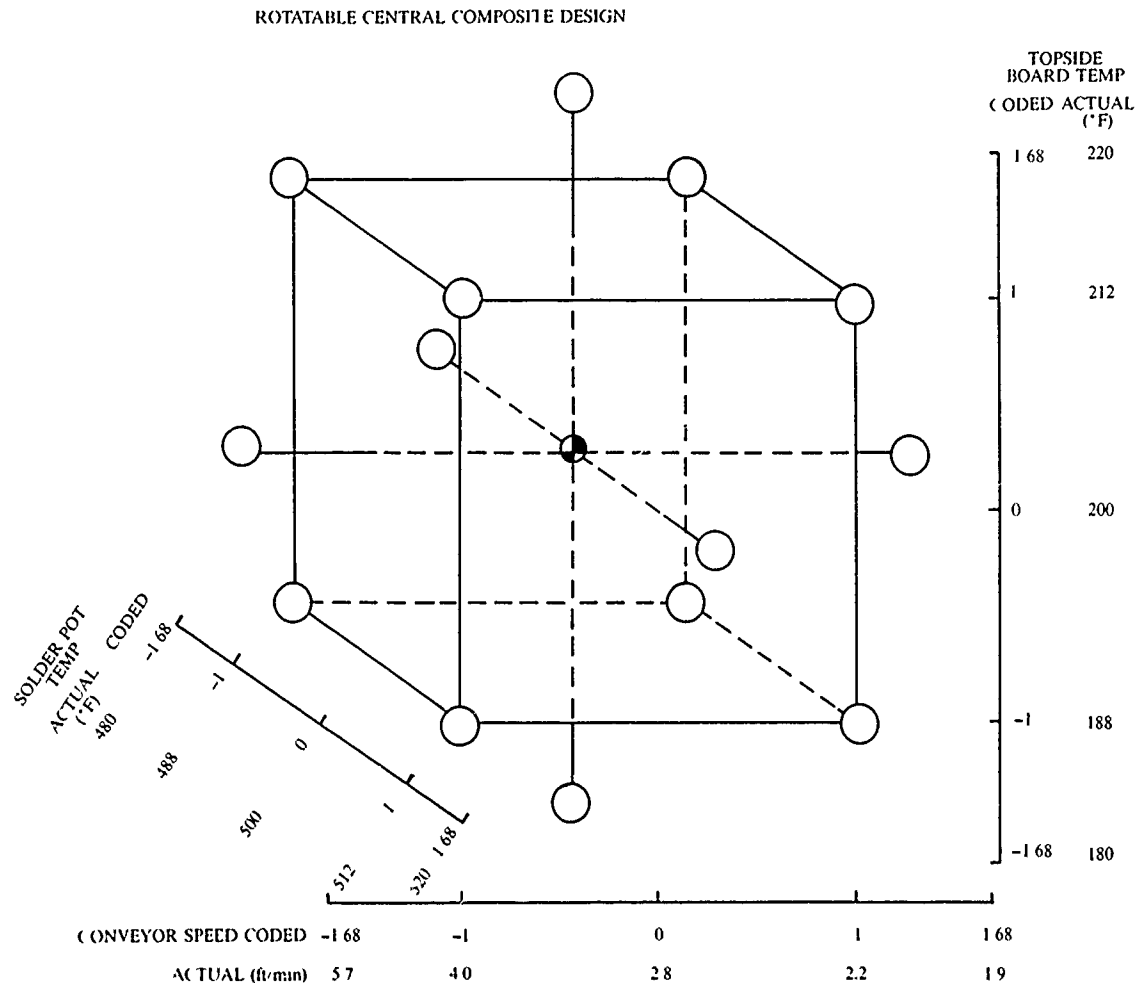
FIGURE 1. Coded Factor Levels/Actual Factor Levels.

The experimental run order was randomized with the restriction that runs with equal solder pot temperature be in groups of 4 for Experiment #1 and in groups of 2 for Experiment #2. Randomizing run order helps protect against any unknown and/or uncontrolled source of bias. It also provides a true estimate of process variability. While complete randomization is ideal, it is believed grouping solder pot temperature did not adversely affect the variance estimate. The boards, identified by serial number, were randomly assigned to the experimental runs. The factor level combinations in run order for Experiments #1 and #2 are listed in Tables 2 and 3.

TABLE 2. Wave Solder Optimization Experiment. Rotatable Central
Composite Design. Factor Level Combinations.

(Design A: Solder Temp Grouped)

Part No 656-4045-001

Run No.	Board Temp (°F)	Conv. Speed (ft/min)	Solder Temp (°F)	PWB S/N
1	188	3.5	488	414
2	212	3.5	488	422
3	188	2.2	488	425
4	212	2.2	488	421
5	200	2.8	480	722
6	200	1.9	500	532
7	220	2.8	500	708
8	200	2.8	500	719
9	180	2.8	500	423
10	212	2.2	512	707
11	212	3.5	512	721
12	188	3.5	512	316
13	188	2.2	512	415
14	200	2.8	500	706
15	200	5.7	500	416
16	200	2.8	500	392
17	200	2.8	520	424

TABLE 3. Wave Solder Optimization Experiment, Rotatable Central
Composite Design. Factor Level Combinations.

(Design B: 7 Center Points)

Part No 643-6128-002

Run No.	Board Temp (°F)	Conv. Speed (ft/min)	Solder Temp (°F)	PWB S/N
1	212	4.0	512	90367
2	212	2.2	512	90258
3	200	2.8	500	90265
4	200	5.7	500	90366
5	200	2.8	500	90372
6	200	2.8	480	90263
7	200	1.9	500	90261
8	200	2.8	500	90374
9	212	4.0	488	90267
10	188	4.0	488	90368
11	200	2.8	500	90264
12	220	2.8	500	90369
13	200	2.8	520	90259
14	180	2.8	500	90266
15	200	2.8	500	90370
16	188	2.2	488	90257
17	212	2.2	488	90262
18	188	4.0	512	90371
19	188	2.2	512	90373
20	200	2.8	500	90260
21	200	2.8	500	90375

The effect of changes in the parameters (response) was measured by evaluating the incidence of defects in eight categories. Note that this inspection was not done per any assembly specification. The intent was to record any deviation from nominal which could be attributed to the wave soldering process. The PWBs were inspected at 10X, and deviations from ideal (as opposed to nonconformance to specification requirements) for the following eight defect categories were recorded:

1. Plated through-holes not completely filled
2. Nonwet/dewet components
3. Peaks/points/icicles
4. Voids/pin holes/blow holes
5. Bridging
6. Nonwet/dewet printed wiring board
7. Insufficient solder in joint
8. Grainy solder

RESULTS FOR EXPERIMENT #1 — PART NUMBER 56-4045-001

These boards were scrap which had been in storage for some undefined period of time. They were populated with components which were also scrap. The component density on the boards was relatively light, with no massive components or connectors.

Even with the relatively poor solderability of the components and boards used, five categories had defect levels so low that a statistical analysis would not be meaningful. The categories were:

- voids/pinholes/blowholes
- bridging
- nonwet/dewet pwb
- plated through holes not completely filled
- grainy solder

The remaining three defect categories (plated through-holes not completely filled, nonwet/ dewet components, and peaks/points/icicles) had defect rates high enough to fit to a mathematical model.

Contour plots, showing defect levels as a function of time and topside board temperature for a constant solder pot temperature, are given in Figures 2 through 10. Contour plots were plotted for 480, 490, 495, 500, 505, 510, and 520 °F solder pot temperature to determine optimum settings. Plots of solder pot temperature of 500 °F contained the largest overlapping area of low defects for both plated through holes not completely filled and nonwet/dewet components. The extreme solder temperatures of 480 °F and 520 °F consistently had higher defects than the mid-range temperatures. Plots for 495 °F and 505 °F were similar to, but not better than 500 °F. For these reasons and in the interest of simplicity, contour plots for 490 °F, 500 °F and 510 °F only are included in this report.

List of Contour Plots for Experiment #1

Holes Not Filled	Solder Temp = 490 °F	Figure 2
Holes Not Filled	Solder Temp = 500 °F	Figure 3
Holes Not Filled	Solder Temp = 510 °F	Figure 4
Nonwet/Dewet Components	Solder Temp = 490 °F	Figure 5
Nonwet/Dewet Components	Solder Temp = 500 °F	Figure 6
Nonwet/Dewet Components	Solder Temp = 510 °F	Figure 7
Peaks/Points/Icicles	Solder Temp = 490 °F	Figure 8
Peaks/Points/Icicles	Solder Temp = 500 °F	Figure 9
Peaks/Points/Icicles	Solder Temp = 510 °F	Figure 10

NOTE: The scales on the contour plots were extended slightly beyond the range of factor levels used in the experiment. This means the edges of the contour plots are extrapolated slightly beyond the experimental region.

FIGURE 2. Holes Not Filled (Exp 1)
Solder Pot Temp = 490 °F.

FIGURE 3. Holes Not Filled (Exp 1)
Soider Pot Temp = 500 °F.

FIGURE 4. Holes Not Filled (Exp 1)
Solder Pot Temp = 510 °F.

FIGURE 5. Nonwet/Dewet Components (Exp 1)
Solder Pot Temp = 490 °F.
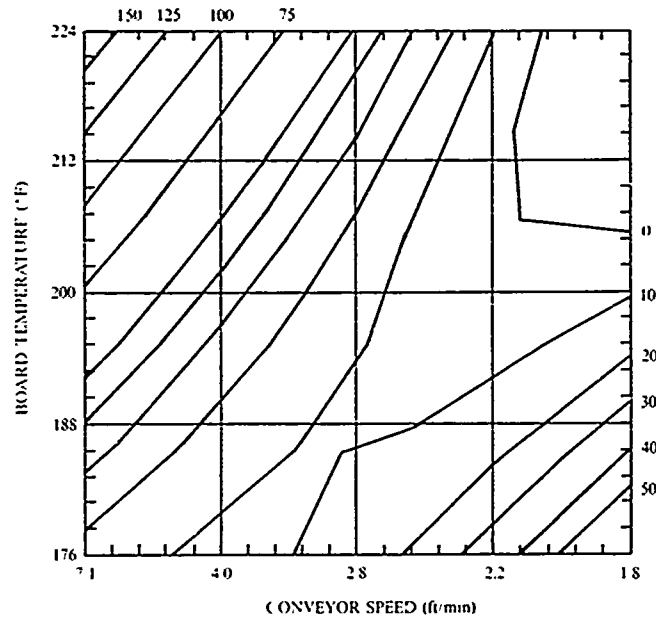
FIGURE 6. Nonwet/Dewet Components (Exp 1)
Solder Pot Temp = 500 °F.
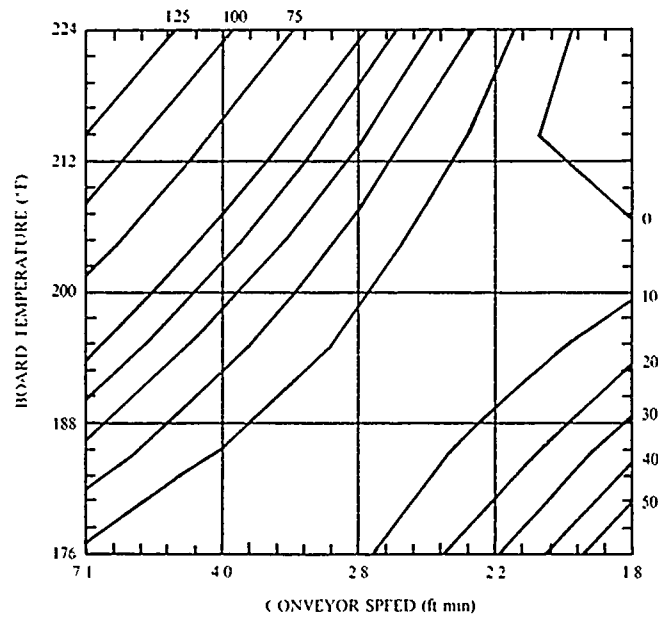
FIGURE 7. Nonwet/Dewet Components (Exp 1)
Solder Pot Temp = 510 °F.
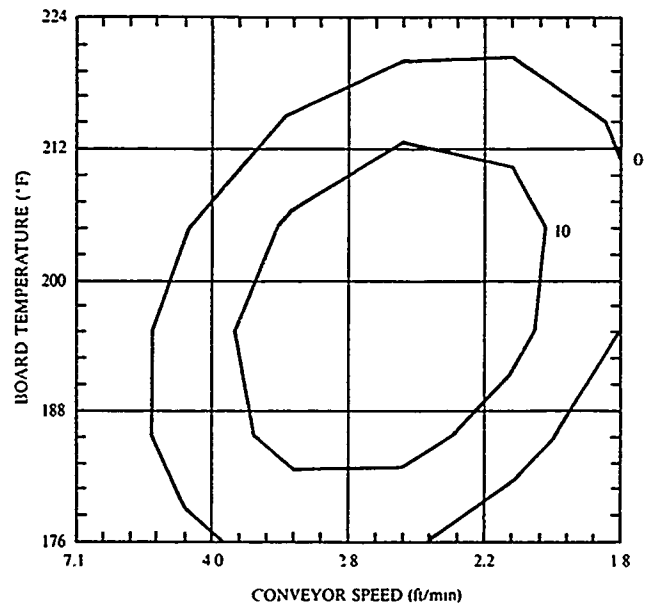
FIGURE 8. Peaks/Points/Icicles (Exp 1)
Solder Pot Temp = 490 °F.
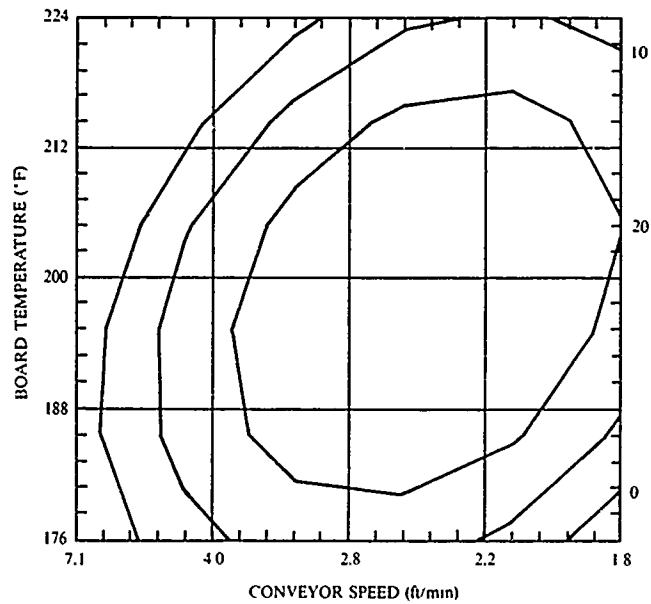
FIGURE 9. Peaks/Points/Icicles (Exp 1)
Solder Pot Temp = 500 °F.
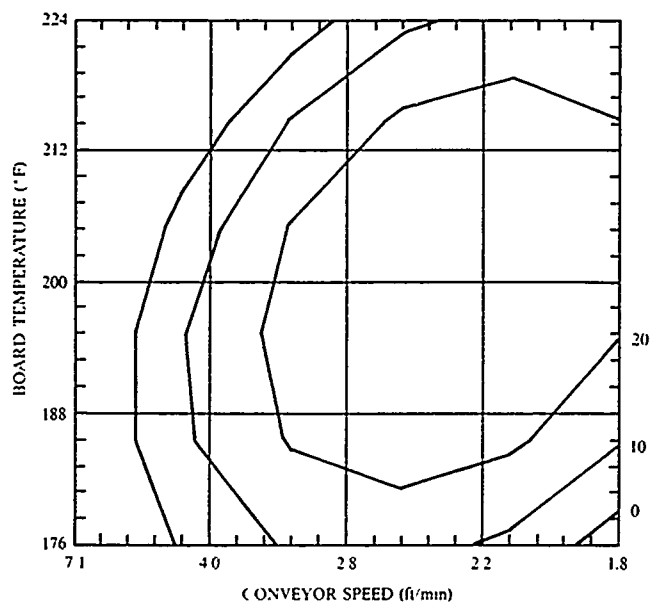
FIGURE 10. Peaks/Points/Icicles (Exp 1)
Solder Pot Temp = 510 °F.

CONCLUSIONS FOR EXPERIMENT #1

Plated Through Hole Not Completely Filled

The predicted minimum value of 4 occurs at:

Solder Temp = approx 495 °F
Board Temp = approx 200 °F
Conveyor Speed = approx 1.9 ft/min

Nonwet/Dewet Components

Nonwet/Dewet Components has a rather flat plain with low defects at solder temperature = 510 °F and conveyor speed less than 3.5 ft/min. See Figure 7 for the exact shape. However, there is a region of low defects at solder temperature = 500 °F that is compatible with a large area of low defect for holes not filled (see Figure 6).

Peaks/Points/Icicles

Unfortunately, the maximum for peaks/points/icicles occurs in the same vicinity as the minimum for plated through holes not filled.

The predicted maximum value of 34 defects occurs at:

Solder Temp = approx 505 °F
Board Temp = approx 200 °F
Conveyor Speed = approx 2.4 ft/min

The high values noted for this defect indicated that there was a problem with the solder wave velocity on the exit side of the wave. In order to reduce the overall incidence of peaks/points/icicles, a mechanical adjustment was made in the height of the dam on the exit side of the wave after Experiment #1. The change did reduce the incidence to an insignifican t level for all conditions which were tested. This was verified in Experiment #2.

SUMMARY FOR EXPERIMENT #1

The region most likely to include the optimum for all defect types, excluding points/peaks/icicles, is illustrated in Figure 11. Thirty defects were chosen as the boundary for the optimum region for holes not filled and 25 as the boundary for the optimum region for nonwet/dewet components, because 25/30 is the smallest defect level that can be clearly differentiated from zero, given the background noise. The best estimate for optimum settings for PWB Part No. 656-4045-001 is:

Solder Temperature = 500 °F
Board Temperature = 200 - 205 °F
Conveyor Speeds = 2.2 - 2.4 ft/min
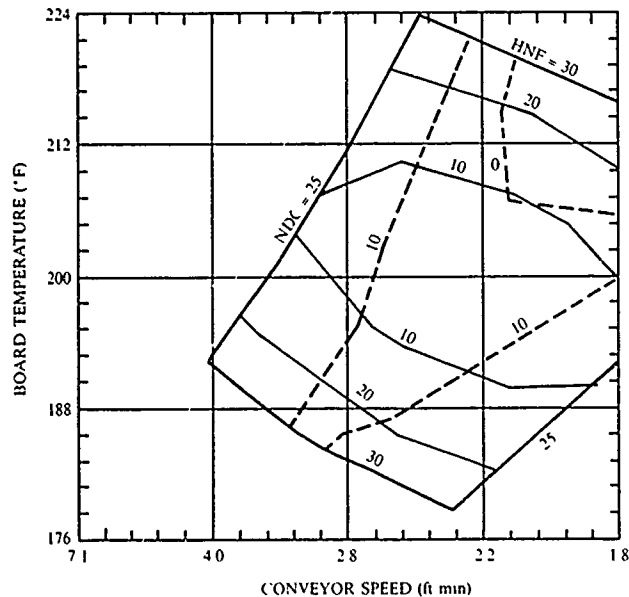
FIGURE 11. Simultaneous Optimization of Holes Not Filled and
Nonwet/Dewet Components
Solder Pot Temp = 500 °F.

RESULTS FOR EXPERIMENT #2 - PART NUMBER 643-6128-002

Twenty-one production PWBs were used to repeat the experiment. Seven center points, instead of three, were run to provide a better estimate of process variability. The PWBs used in this case had a much greater thermal mass than those used in the first run and also had a much higher component density. Again the boards were inspected at 10X, for deviations from ideal, not to normal production inspection standards.

The overall defect level for the second experiment was lower than that of the first. In order to do a statistical analysis, insufficient solder, nonwet/dewet components, and nonwet/dewet PWB were combined into one category.

Four defect categories had defect levels that were zero or near zero over the entire factor space. They were:

Peaks/points/icicles (note improvement from Experiment #1)
Bridging
Voids/pinholes/blowholes
Grainy solder

Holes not filled and insufficient solder (including nonwet/dewet PWB and nonwet/dewet component) had defect rates high enough to analyze.

Contour plots for Experiment #2 are shown in Figures 12 through 21. Plots at all five temperatures are shown for holes not filled and insufficient solder.

Contour Plots for Experiment #2

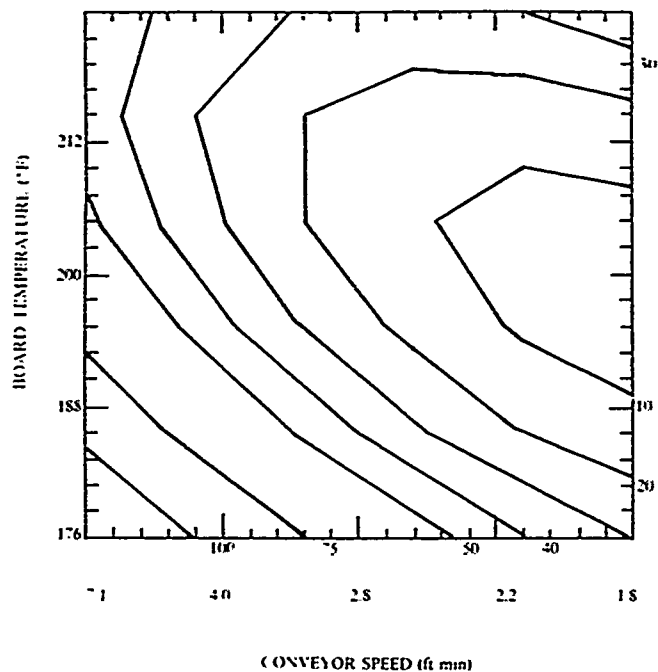| Holes Not Filled | Solder Temp = 480 °F | Figure 14 |
Holes Not Filled	Solder Temp = 490 °F	Figure 15
Holes Not Filled	Solder Temp = 500 °F	Figure 16
Holes Not Filled	Solder Temp = 510 °F	Figure 17
Holes Not Filled	Solder Temp = 520 °F	Figure 18
Insufficient Solder	Solder Temp = 480 °F	Figure 19
Insufficient Solder	Solder Temp = 490 °F	Figure 20
Insufficient Solder	Solder Temp = 500 °F	Figure 21
Insufficient Solder	Solder Temp = 510 °F	Figure 22
Insufficient Solder	Solder Temp = 520 °F	Figure 23
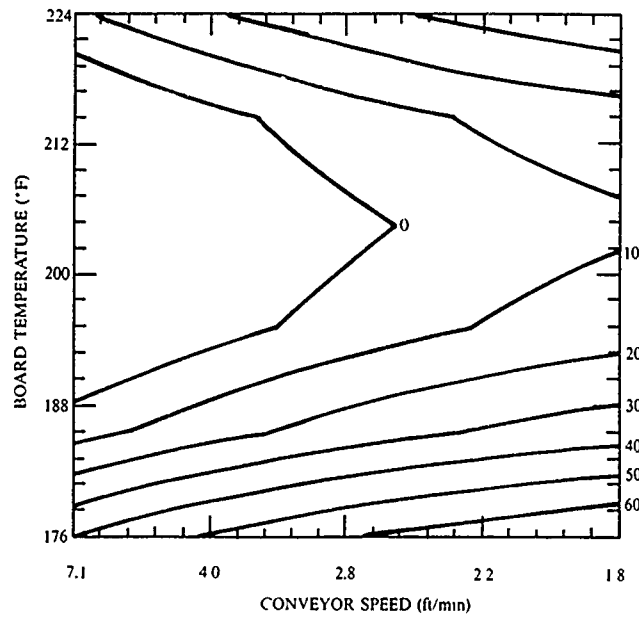
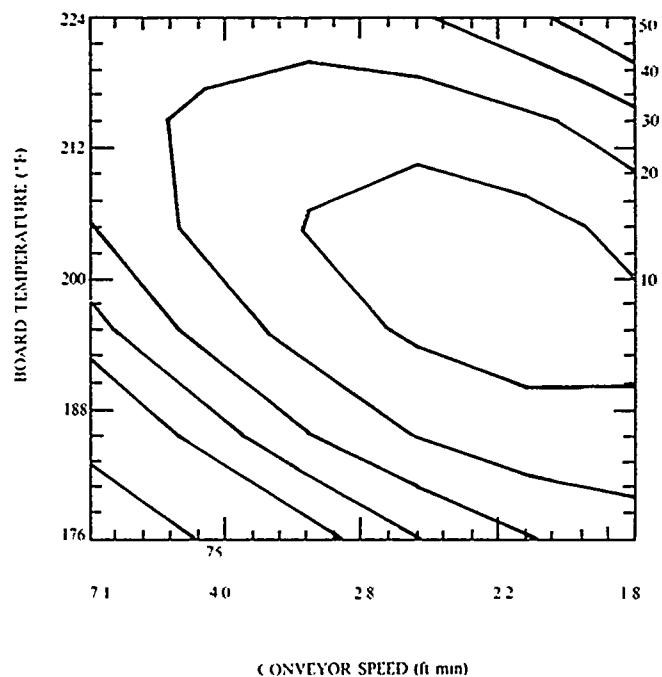FIGURE 12. Holes Not Filled (Exp 2)
Solder Pot Temp = 480 °F.
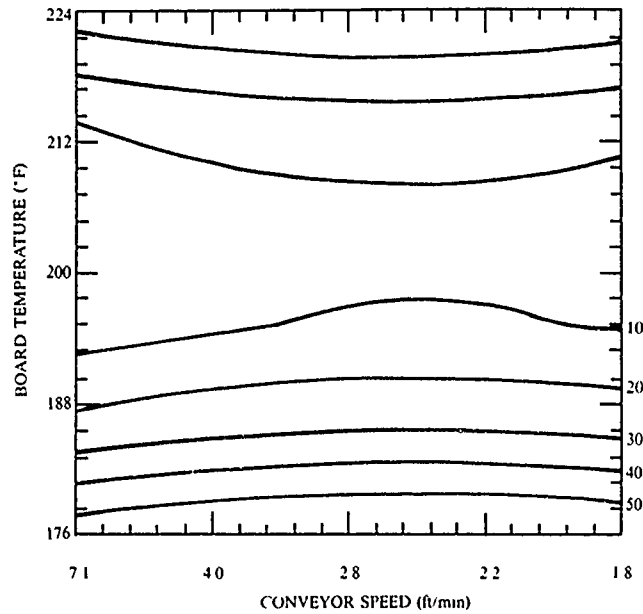
FIGURE 13. Holes Not Filled (Exp 2)
Solder Pot Temp = 490 °F.
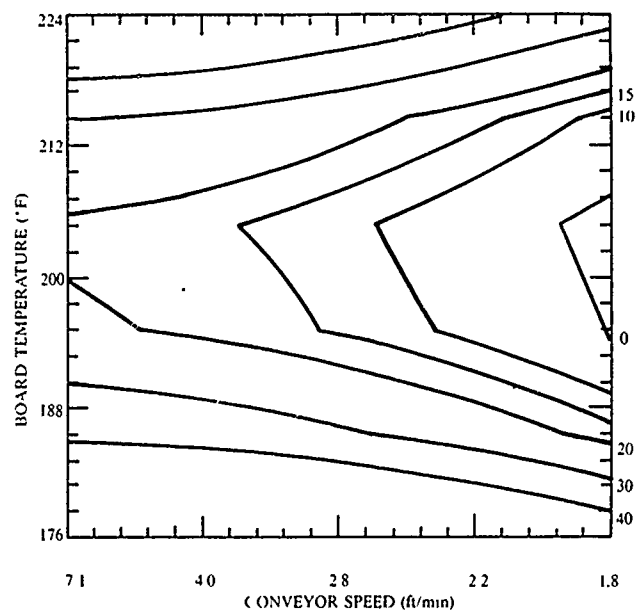
FIGURE 14. Holes Not Filled (Exp 2)
Solder Pot Temp = 500 °F.
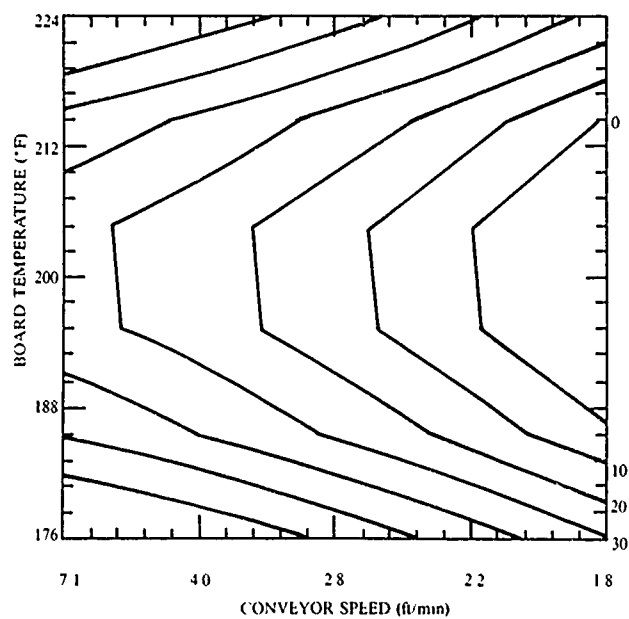
FIGURE 15. Holes Not Filled (Exp 2)
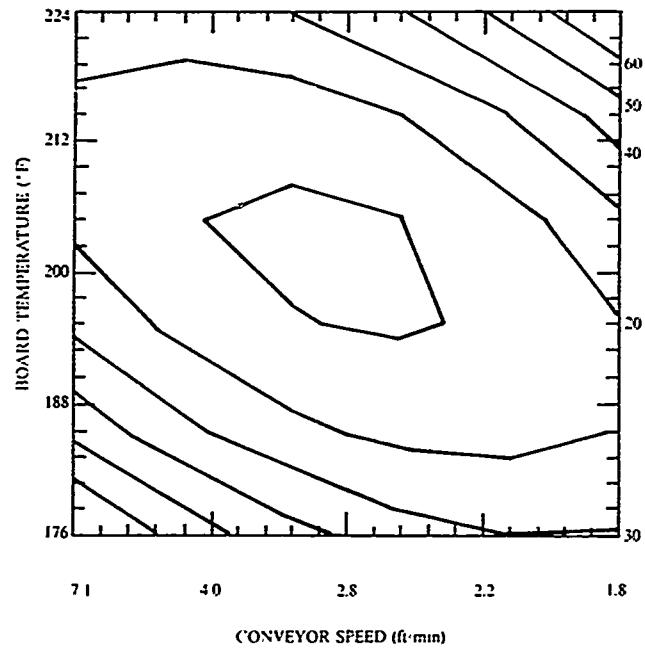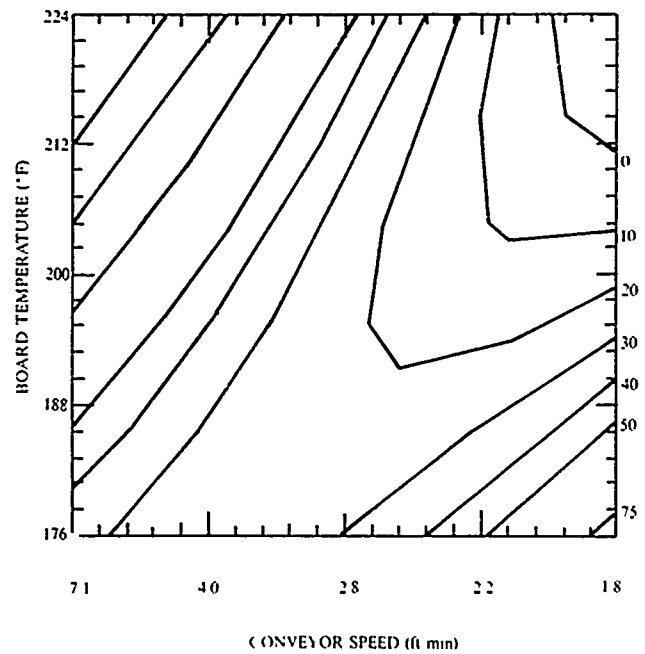Solder Pot Temp = 510 °F.
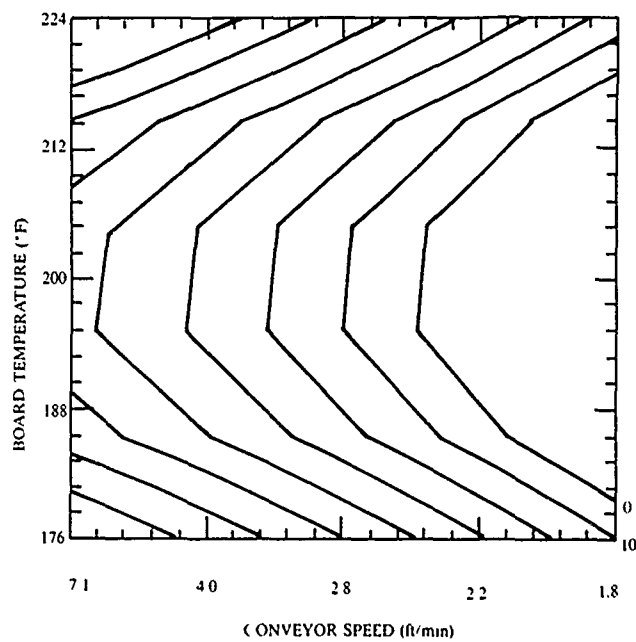
FIGURE 16. Holes Not Filled (Exp 2)
Solder Pot Temp = 520 °F.
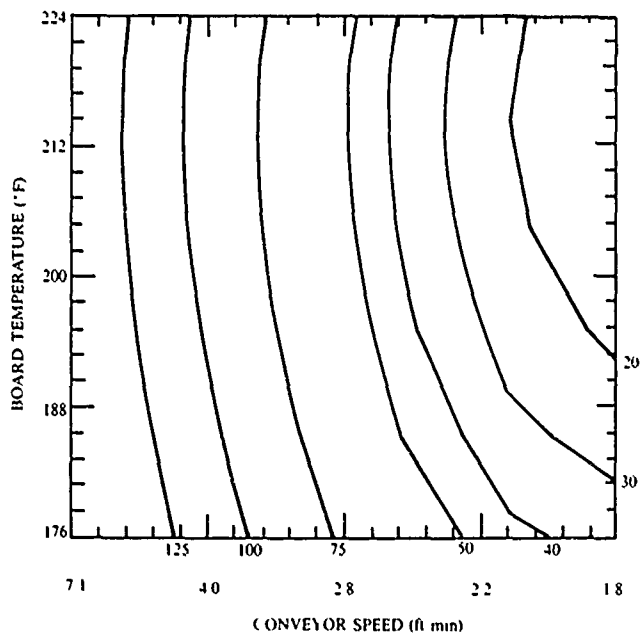
FIGURE 17. Insufficient Solder (Exp 2)
Solder Pot Temp = 480 °F.
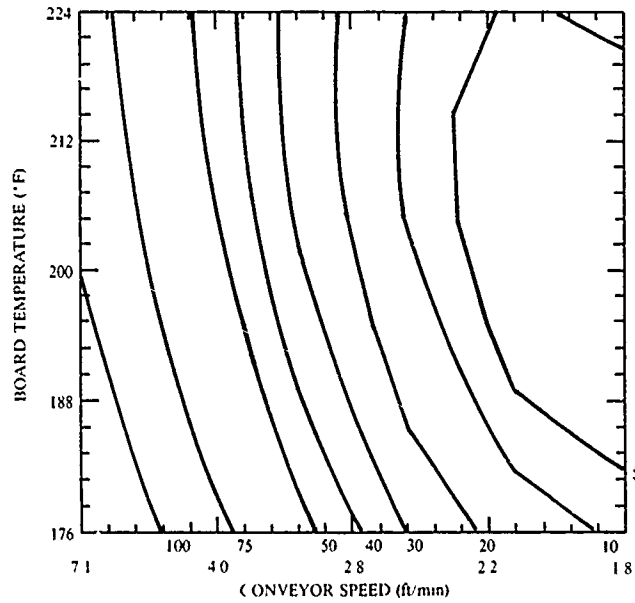
FIGURE 18. Insufficient Solder (Exp 2)
Solder Pot Temp = 490 °F.
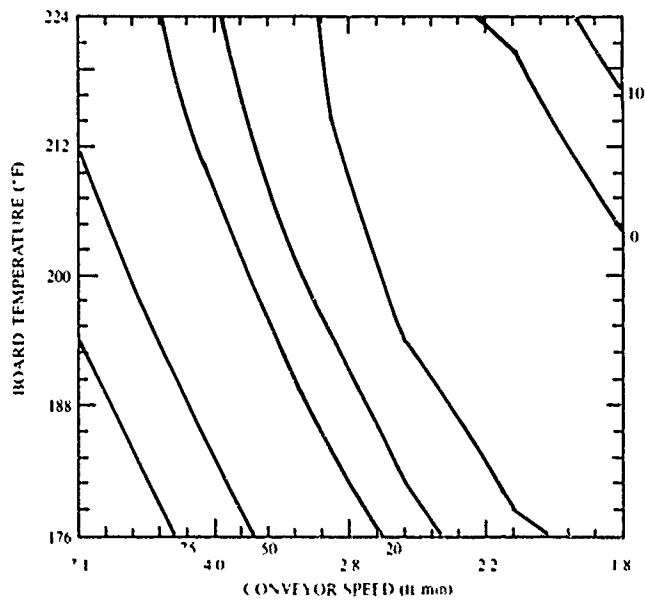
FIGURE 19. Insufficient Solder (Exp 2)
Solder Pot Temp = 500 °F.
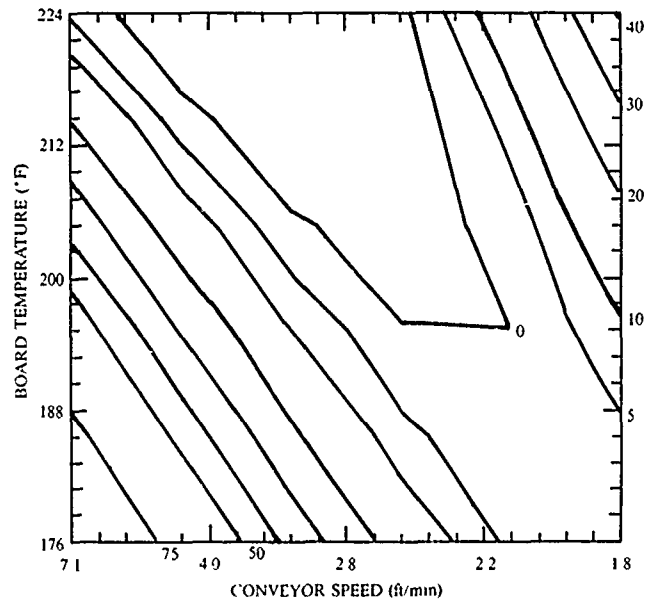
FIGURE 20. Insufficient Solder (Exp 2)
Solder Pot Temp = 510 °F.
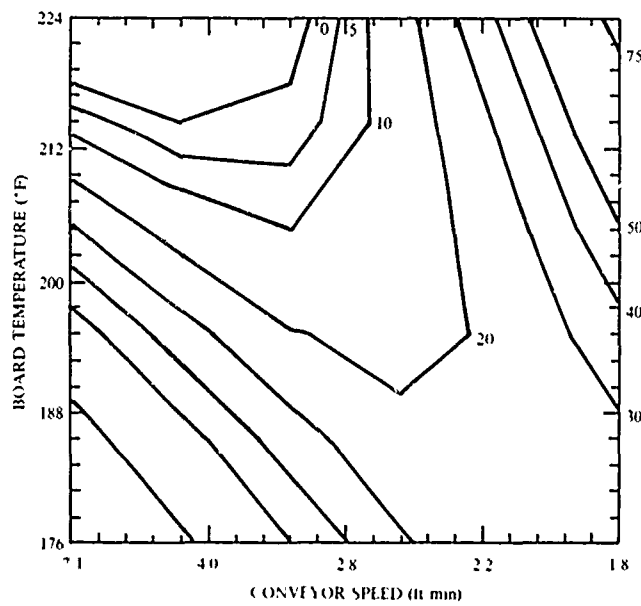
FIGURE 21. Insufficient Solder (Exp 2)
Solder Pot Temp = 520 °F.

CONCLUSIONS FOR EXPERIMENT #2

Holes Not Completely Filled (HNF)

This defect has a saddle point at:

Solder temperature = 490 °F
Board temperature = 200 °F
Conveyor Speed = 2.0 ft/min

The largest areas of zero predicted defects for HNF occurs at 480 °F and 520 °F. However, at these temperatures, insufficient solder has a very high defect level for the same time and board temperature conditions that produce low HNF defects.

Insufficient Solder

Insufficient solder has a minimum at:

Solder temperature = 500 °F
Board temperature = 210 °F
Conveyor Speed = 2.3 ft/min

SUMMARY FOR EXPERIMENT #2

The largest area of overlapping minimums for holes not filled and insufficient solder occurs at 500 °F solder pot temperature. It is pictured in Figure 22.

Boundaries for the optimum region are 20 for holes not filled and 15 for insufficient solder. These defect levels are the lowest that are significantly different from zero. That is, the noise level for zero defects extends to 20 for Holes Not Filled and 15 for Insufficient Solder. Note this data is "less noisy" than that for Experiment #1.
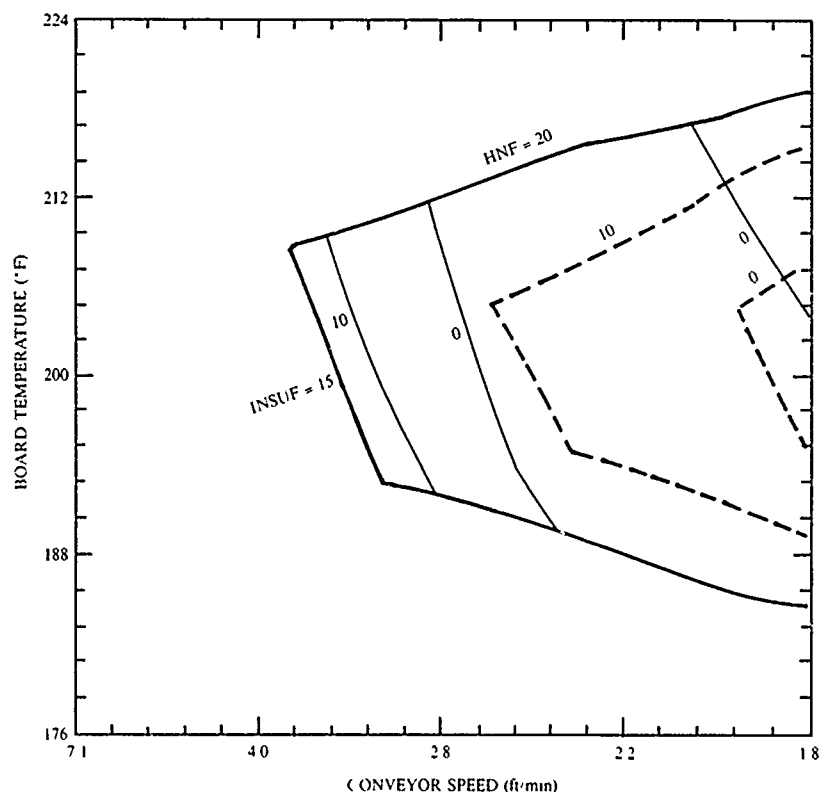
FIGURE 22. Simultaneous Optimization of Holes Not Filled and Insufficient Solder
Solder Pot Temp = 500 °F.

SUMMARY OF COMBINED RESULTS

Figures 11 and 22, the simultaneous optimization of defect categories for Experiments #1 and #2, indicate a rough "95% confidence" region for the optimum. The best estimate for the optimum for each experiment is:

Experiment #1

       Solder Pot Temperature = 500 °F
       Topside Board Temperature = 200 °F
       Conveyor Speed = 2.1 ft/min

Experiment #2

       Solder Pot Temperature = 500 °F
       Topside Board Temperature = 200 °F
       Conveyor speed = 1.9 ft/min

The area common to the optimum areas for Experiments #1 and #2 is pictured in Figure 23. The dashed inner circle indicates the area where predicted defect levels for both defect categories for both experiments are less than or equal to ten.
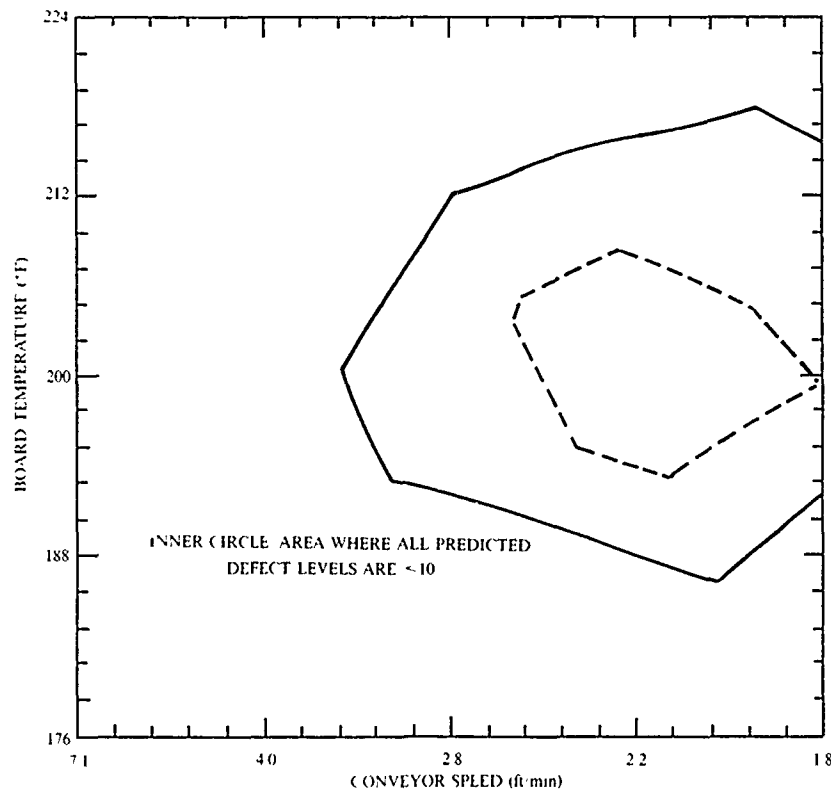
FIGURE 23. Overlap of Optimum Area (Exps 1 & 2)
Solder Pot Temp = 500 °F.

CONCLUSIONS

Statistical Experimental Design provides a powerful tool for accurately characterizing complex processes. In the specific example considered here, the statistical design and data analysis shows not only the optimum operating parameters, but the size of the operating "window" around the optimum parameter settings. This information can be used in turn to design a rational statistical process control plan which can be expected to keep the defect rate down to the level which the experiment showed it was possible to achieve.

ACKNOWLEDGMENTS

The author is grateful to Elizabeth Morgan of Collins Defense Communications, Richardson, Texas, for the detail statistical work on which this paper is based.

REFERENCES

1. R. A. Fischer. *Statistical Methods for Research Workers*, Oliver and Boyd, 1935.

2. DuPont Riston Products Division, *Strategy of Experimentation*, Revised Edition, October 1986.

3. Box, Hunter, Hunter, *Statistics for Experimenters*, Wiley, 1978.

4. K.M. Lin. "Optimizing the Wave Solder Process", in *Electronic Packaging and Production*, February 1986. Pp 108-115.

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INFRARED FEEDBACK FOR REAL-TIME
CONTROL OF LASER SOLDERING

by

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ABSTRACT

Lasers have been in use for many years in performing open-loop
reflow soldering by the use of predetermined doses of radiation. We
have investigated the use of closed-loop laser reflow soldering to
handle cases where the heat requirements of individual joints may
vary. An infrared detection system monitors the surface temperature
of each solder joint during heating. When a predetermined threshold
is reached, the laser-beam shutter is placed in a dither mode so as
to stabilize the target surface temperature until the heat has
penetrated the entire mass. Thermal signatures are displayed as
temperature-vs-time plots; when these are alike, they indicate that
joints of similar quality are being formed. Signatures whose features
differ from the normal ones indicate improperly prepared joints
which can cause ringing of the control function or premature shut-
down due to overheating.

INTRODUCTION

Recent decades have witnessed the progressive automation of
electronic circuit board production until nearly all manufacturing
operations have become automated. The last process to be automated
was the inspection of the product before it leaves the line.

Until now the main purpose of inspection has been to find
defects brought about by soldering so that they can be repaired or
reworked. Lately, a more compelling reason for inspection is to
identify and to correct any production process problems which may be
the sources of defects so that these will not occur in the first place.

This paper describes a procedure which makes use of a laser and
an infrared detector in order to combine the soldering and inspection
steps into one. The concept is based on the laser-heating of the
solder material (paste, preform, etc.) until melting ("reflow") is

observed by the infrared detector. At this point, the laser beam is
interrupted, having delivered the proper heating energy regardless
of the size of the joint. The joint's thermal history, as seen by
the detector, is its "inspection Certificate", containing pertinent
information about the physical properties of the newly formed joint.
Thermal histories which are repeatable indicate consistency in the
quality of the soldering process.

Although the solder joints are presently formed on a one-at-a-
time basis, the somewhat longer manufacturing time compared to other
processes is partly compensated for by the elimination of a separate
inspection process. Moreover, in cases where joints of intentionally
different sizes occur on the same circuit board, each one receives
a tailored amount of reflow energy, thus avoiding the underheating or
overheating which occur when the entire board is soldered at once.

Further potential savings arise as a result of the real-time
availability of process control data which make possible the rapid
correction of process anomalies.

THE LASER/INSPECT SYSTEM

The forerunner to the soldering-and-inspection machine was the
Laser/INSPECT system, an inspection-only system introduced by our
Company in 1982 for the circuit board manufacturing industry
(Reference 1). At that time, the visual inspection of solder joint
quality was the last manual process waiting to be automated. The
intent of Laser/INSPECT was to eliminate the cost and the subjectivity
of the human operation and the known tendency of inspectors to make
errors of judgment; a second objective was to increase the inspection
rate.

Industry studies have revealed the inconsistency of judgment of
human inspectors. A recent one (Reference 2) showed that one in-
spector, in examiming the same printed circuit board at two different
times, agreed with himself in only 44% of the cases, as seen in
Figure 1. Two inspectors agreed with each other in 28% of the cases,
three agreed on 12% and four agreed on 6% of the cases.

At present, more than three dozen Laser/INSPECT systems are in
operation here and abroad, inspecting solder joints at rates up to ten
per second. Their use on the production floor has been widely
described by manufacturers of military and consumer products, as in
References 3 through 7.

In operation, a timed pulse of a focused laser beam impinges on
the surface of each target where part of it is absorbed and is
converted to heat. The rate at which the heat dissipates into the

SOLDER JOINT
VISUAL INSPECTION
OF THE SAME P.C. BOARD

44%	28%	12%	6%
1 INSPECTOR	2 INSPECTORS	3 INSPECTORS	4 INSPECTORS

SHADED AREAS: % OF AGREEMENT

BLANK AREAS: % OF DISAGREEMENT

COURTESY: AT+T, BURLINGTON, N.C.
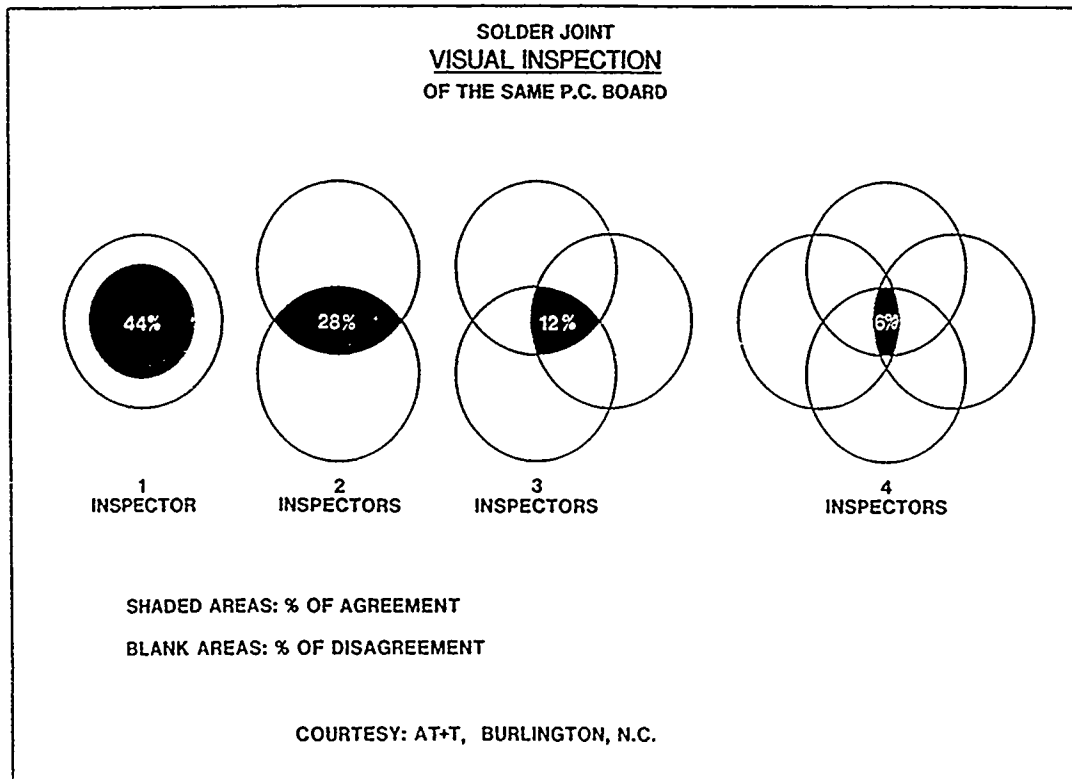
FIGURE 1.   Inconsistency of Human Inspection Results
on Solder Joints.

interior is a measure of the amount of thermal mass beneath or around
the target point; the greater the mass, the less is the surface
heating seen by an infrared detector focused at the target point.   An
electrical lead at an intended lap joint, for example, which is not
connected to the solder pad underneath will become much warmer than
a bonded lead.   Moreover, an intact solder joint which is discolored,
contaminated, porous or pitted will exhibit greater laser-beam
absorptance (as well as infrared emittance) than a clean, shiny
surface and will register a higher infrared signal.

The thermal histories, or "infrared signatures", of a few
joints of various qualities are depicted in Figure 2.   In the
particular case of the uppermost curve, the burnoff of some com-
bustible contaminant caused a steep initial rise in the heating
curve, followed by a sudden drop when the shutter closed, in-
dicating an intense but superficial heating condition.

A block diagram of the inspection system appears as Figure 3.
The heating source is a neodymium-doped, yttrium-aluminum-garnet

FIGURE 2. (right). "Dictionary"
of Infrared Signatures of a
Family of Solder Joints.
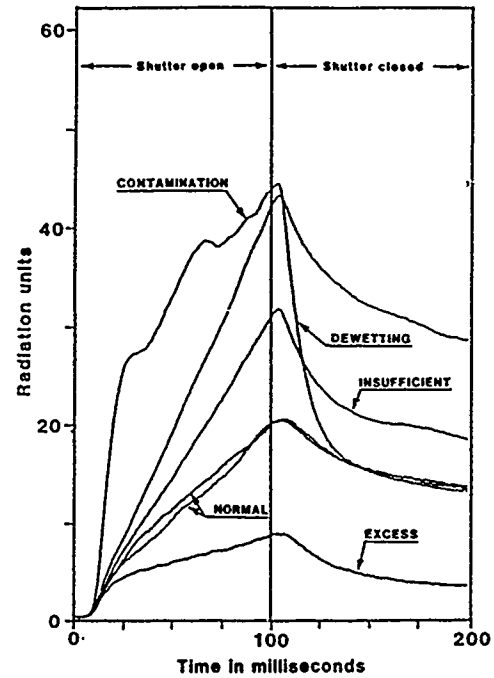
FIGURE 3 (below). Block
Diagram of the Laser/
Thermal Inspection Concept.
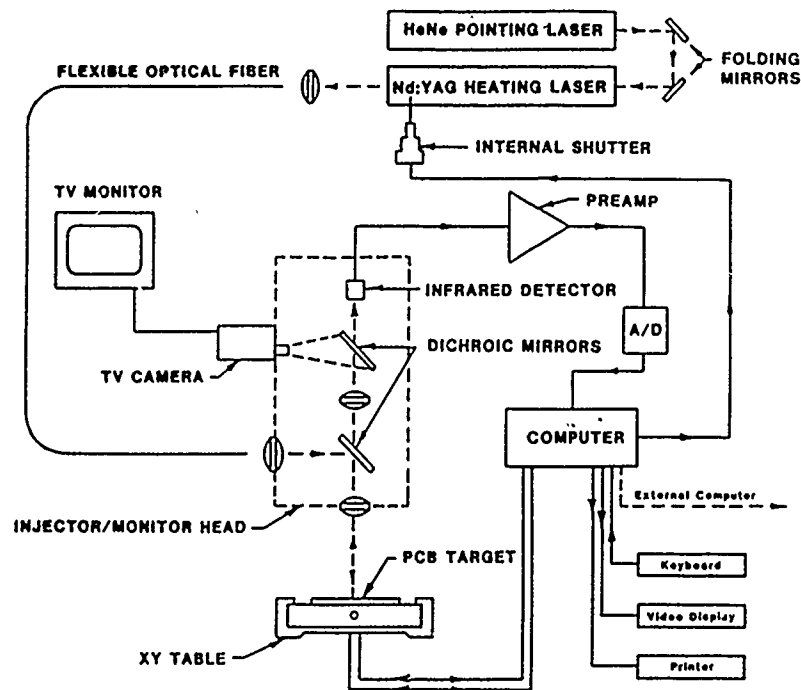
(Nd:YAG) laser rated at thirty watts but most often used at a lower power level. Its emitted invisible beam consists of a narrow spectral band of infrared wavelengths centered at 1.06 μm (micrometers), where 1 μm is one-millionth of a meter. When focused to a half-millimeter-diameter spot, as is done here, it has a heating capability greater than that at the surface of the sun. A typical exposure duration of twenty milliseconds will warm the surface of a clean, shiny solder joint by 25 to 50 Centigrade degrees above its initial temperature. A detached lead or a non-shiny surface will get considerably hotter.

For visual targeting purposes, the laser beam is made visible by the addition of a half-milliwatt of red light from a helium neon (HeNe) laser. Alternatively, the programming of target positions is carried out with the aid of a closed circuit television system whose camera is shown at the injector/monitor head.

Both laser beams are focused into a flexible optical fiber of just over a half-millimeter diameter. This serves to homogenize the power density distribution over the beam cross section, for laser beams are highly irregular in this regard. The fiber also provides vibration isolation between the lasers and the vigorous movements of the XY positioning table.

Within the injector/monitor head, a lens and mirror system brings together the axes of the laser beams, the infrared detector and the television camera so that all are focused at the target point. The infrared detector is an InSb (indium antimonide) cell cooled to 77°K and operating in the photovoltaic mode. Before it is an optical blocking filter which obstructs reflected laser-beam rays so that they will not be confused with the longer infrared wavelengths arising from the heated targets.

A central item in the system is the Digital Equipment Corporation video terminal with microcomputer which controls the inspection sequence and processes the resulting thermal data. Target positions are preprogrammed, shutter timing is controlled, and digitized thermal readings are compared with those previously stored in memory arising from "learning session" inspection of known good joints.

LASER SOLDERING AND INSPECTION

Early in the development of the system, it was observed that solder joints under laser/thermal inspection could easily be reflowed if the shutter were inadvertently left open for too long. Reflow was marked by a jog in the heating curve due to the well known latent heat of fusion phenomenon. This is the condition in which heating energy is extracted from the beam at the moment of melting, with no

resultant temperature increase. Instead, the energy is applied to the breaking of the cohesive bonds which had held the tin and lead atoms in solid form. Afterward, during resolidification or freezing, a jog appears in the cooling curve as the atoms again join and release the borrowed energy.

In principle, the computer could be made to recognize both jogs via mathematical differentiation. It could use the first jog as a signal to close the laser shutter. The second jog would announce that it is safe to accelerate the table to the next target position without disturbing any molten solder.

In practice, this is not always easy to do for the jogs are often not very distinct. This is seen in Figure 4 where the second jog, at the moment of freezing, is rather subtle. The first jog,
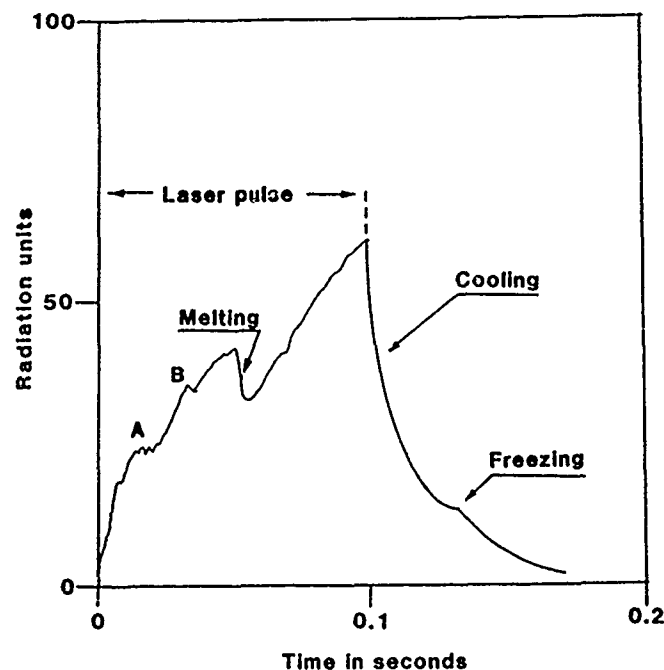
FIGURE 4. Analysis of Infrared Signature Developed During Soldering.

during melting, is artificially enhanced because the material being reflowed is solder paste. This is a grayish, granular mass of solder particles combined with flux and, before liquefying, exhibits high absorptance and emittance. The heating irregularities at Points A and B are due to local areas of paste beginning to melt before the entire mass is reflowed. Major melting occurs at the

first arrow. The steep drop in radiated power occurs when the gray
paste turns molten and shiny, with a consequent drop in emittance.

Had the reflowed material been a solder pad or a preform, the
melting jog would not be as consipicuous.

Because of the uncertainty of jog detection, we have adopted an
approach based on straightforward temperature measurement and timing.
A temperature threshold is selected on the basis of trial and error.
The temperature is monitored at the part of the solder surface where
the laser beam impinges. It is, of course, much higher here than
elsewhere if the entire solder mass is to reach its reflow tempera-
ture.

Once the threshold temperature has been reached, it is held
there by means of rapid cycling of the laser shutter; this is to allow
the full solder mass to reach its reflow temperature. The shutter
cycles are controlled thermostatically as in a domestic heating
system; that is, there is an upper threshold at which the shutter is
closed and a lower one which opens it. The cycles are counted by
the computer and after a certain number of them (such as four), the
shutter is closed permanently.

The interesting point of this method is that the soldering
process automatically adjusts itself to the heating requirements of
each solder joint, be it large or small, be it well heat-sunk or
poorly so. The self-adjusting feature occurs when the shutter cycle
time adapts itself to the heat demands of the joint. For example, a
small solder mass will cycle more rapidly between its upper and lower
limits than will a large one, and so a short cycle time is the result.
Similarly, a well heat-sunk mass of any size behaves as a large
solder mass, taking longer to warm up and to cool down, thus generat-
ing a longer cycle than a poorly heat-sunk one.

Apropos of soldering durations, we note that laser soldering
allows the joint to remain molten for less time than do wave soldering
or soldering by infrared or vapor phase. The impact is that laser
soldering generates less of an intermetallic compound layer than
do the other methods. Intermetallic compounds are formed as alloys
of components within the solder and the substrate material, be it
the copper wall of a plated-through-hole or the pad material on the
printed circuit board or be it a gold, nickel or other plating over
the substrate material. These compounds have a different crystalline
structure from those of the parent metals, which serves to weaken
them and which can cause premature mechanical failure in a joint.

The layer thickness is dependent upon the temperature of the
molten solder and upon the time during which it remains molten.
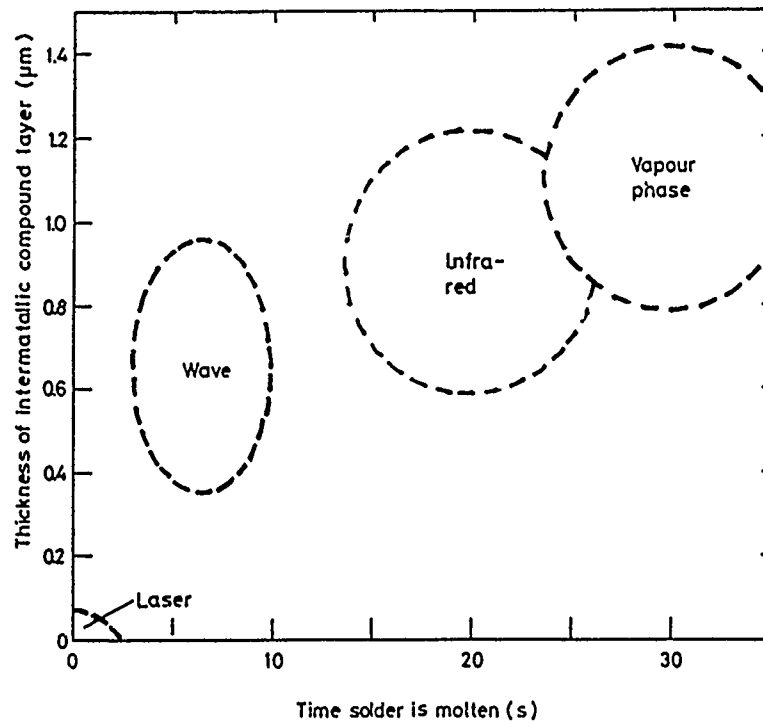
FIGURE 5. Intermetallic Thickness for Different Soldering
Methods.

Figure 5, taken from Reference 8, shows the relationships between
intermetallic thickness and soldering duration for four soldering
methods. It is seen, at the lower left, that the soldering times,
and hence the intermetallic thickness, are less for the laser method
than for the others.

An interesting feature of the self-adjusting process is its
ability to go out of control -- and to notify the operator of this
-- if the soldering conditions are out of its "control band". For
example, let us say that a certain joint failed to be provided with
solder or that its lead was not contacting the pad. The reduced
target mass responds quickly to the application of laser heat; its
temperature rises too rapidly for the shutter to respond in time
and it overheats by the time the shutter has closed. It then
"overcools" before the shutter can open and the large temperature
swings continue until the shutter count has been completed. The
computer is easily taught to recognize the resulting large signal
amplitudes and to signal the presence of a defective joint.

In order to prevent accidental heat damage to a component
or other surface due to inadvertent mistargeting (from operator error
or system malfunction), we have incorporated a "burn prevention"
feature into the system. The detector signal is continuously
monitored and the shutter is prematurely closed when the heating
rate exceeds a predetermined threshold.

Occasionally, a bit of debris or a film of contamination, such
as residual solder flux, will be present on a target surface. These
foreign materials will undergo explosive combustion in the intense
laser-beam heat and can leave charred residue on the target surface.
The burn prevention feature is designed to thwart such damage by
aborting the exposure at the very first sign of runaway heating.
At the same time, the operator is notified by the computer that such
an action has occurred because, effectively, this signifies that a
defect is present.

FIGURE 6. Thermal Signatures
of an Acceptable Solder Joint
and of Two Rejects.
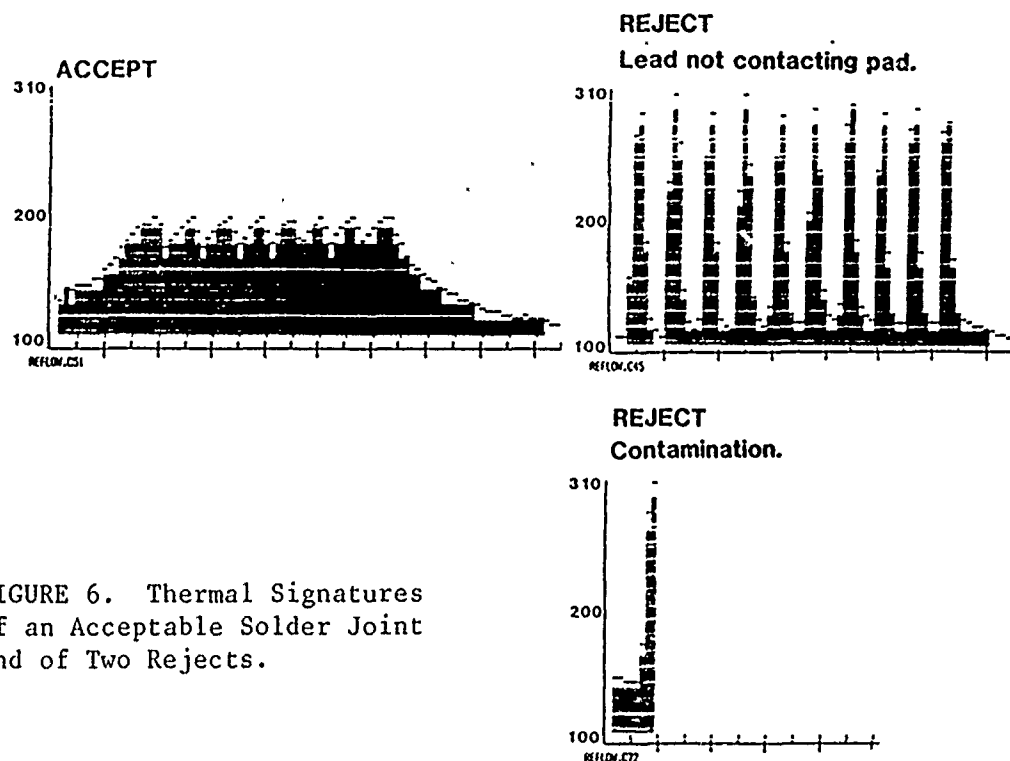
Figure 6 presents some assorted thermal signatures which were recorded during actual laser reflow soldering. These are plots of the infrared signal intensity versus time. The time scales are a few hundred milliseconds in length. They were made artificially long in this case in order to show many thermal cycles for display purposes. Normally, it is desirable to complete the soldering process in as short a time as possible in order to maximize the production throughput as well as to minimize intermetallics formation. For good joints of moderate size, the total soldering time is of the order of one-tenth second.

In the "curve" (the polygonal approximation) for the good bond, the infrared signal is seen to rise steadily to a threshold near 200 thermal units and then to oscillate for several cycles until the shutter is finally closed. In the case of the lead not contacting the pad ("lifted lead"), the initial rise is faster and the signal oscillations are of greater amplitude. Traces such as this are obtained also for deformed and misregistered leads. In the final illustration, the thermal rise was rapid enough to trigger the burn prevention circuit before a second thermal cycle was initiated.

PRACTICAL CONSIDERATIONS

In 1986 a modified Laser/INSPECT system, intended for simultaneous laser soldering and inspection, was introduced under the name ILS 7000 Series Intelligent Laser Soldering System (References 9 through 11). Software was provided for processing the thermal signals for feedback control. The main hardware changes were the addition of an air purge and exhaust system for keeping soldering vapors out of the optical path and of a less sensitive infrared detector (lead sulfide) and amplifier to accommodate the higher temperatures which are achieved in laser soldering. A typical reflow temperature, in the case of 67:33 tin:lead solder, is 183°C. Through the software, the operator has full control over the temperature limits, the number of thermal cycles per joint and so forth.

As an example of the effectiveness of the system, we show in Figure 7 an outline drawing (slightly enlarged) of a printed circuit board which is used in one of our Company products. This is a "mixed technology" board containing both surface-mounted-technology components and pin-in-hole components. The components vary in type and in size; they include chip resistors and capacitors, through-hole IC's, small outline IC's, various transistors, diodes, and so forth. The ratio of largest to smallest target areas is about ten to one.

As a test of the laser soldering system, we are using it for the automatic soldering of all components on this board. The results
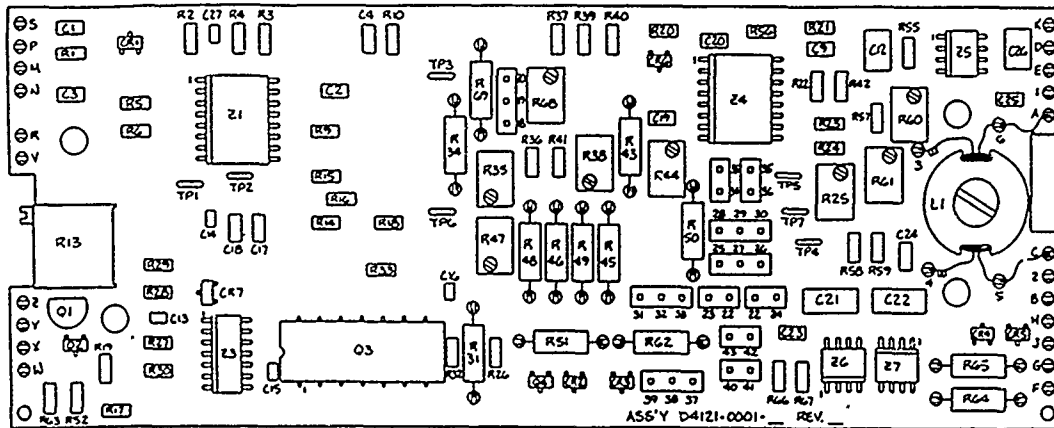
FIGURE 7. A Vanzetti Company Printed Circuit Board Which is
Routinely Soldered by Laser-beam Reflow.

obtained are excellent and surpass those which we would obtain by hand
soldering the board ourselves.

Aside from the system pointing out the presence of an occasional
defect, such as arising from a bit of contamination or from a
deformed lead, the real advantage of the feedback feature is its
ability to detect slow drifts in the quality of the soldering process.
A common process fault is the aging of the solder paste. If one
monitors the thermal signatures, as in Figure 6, he will observe
the process deterioration in the form of a degradation in the
signatures for the acceptable bonds. This takes the form of an
increase in the amplitudes of the thermal swings, and when this
occurs consistently it is the first warning of an impending problem.
We have found this detection method to be highly sensitive to
subtle changes in the solder paste quality. This is because aging
is accompanied by an increase in the absorptance for the laser
beam as well as an increase in the emittance of the thermally
generated infrared radiation. The observed thermal readings are
based not upon absorptance or emittance alone but upon their product.
As a result, process flaws can be detected much sooner by the system
than by eye or any other method.

Other process variables which may drift out of control but
be subject to early detection by our inspection method are the amount
of solder applied to each pad as a result of the screening conditions,
the proper placement of components, the solderability of components,
surface contamination on otherwise solderable components, and so forth.

CONCLUSION

It is apparent that when laser soldering-and-inspection is applied to a group of identically prepared bonds, the resulting thermal signatures should be alike, and if the bonds differ, the signatures will differ; this has been borne out of experiment. One needs merely to instruct the computer as to the range of thermal signature values for acceptable joints in order to have an automatic soldering-and-inspection system.

If we consider the soldering operation alone, this method is slower than the mass-soldering methods, since it solders one joint at a time, at an average speed of 3 to 5 joints per second. But when we consider the joint operations of soldering and inspection, it becomes the fastest of all competing processes, since it does not require a subsequent inspection operation: as soon as a joint is made, its infrared signature (that is, its inspection certificate) is immediately available.

The major advantages offered by the system are:

1. The cost and questionable dependability of human inspection are avoided.

2. Heating is localized at each joint. There is no risk of heat damage to components or other board parts, and built-in safeguards abort the exposures when excessive heating is observed. Thermal stresses in the bonds are reduced.

3. For boards containing various-sized joints, the applied energy requirements of individual joints are taken into account. This avoids overheating of the smaller joints and the possible formation of intermetallic compounds which weaken them.

4. Abrupt increases in the rate of detected defects indicate deterioration in the control of the process so that corrections may be made in near-real-time, thus quickly reducing the occurrence of defects.

5. Densely packed devices are easily soldered without disturbing nearby parts.

6. Because components are soldered one at a time, both sides of a board may be populated.

7. Intermetallic compound formation is minimized, resulting in shiny and less brittle joints.

8. The rapid solidification results in a fine microstructure, improving low-cycle fatigue properties.

9. There is no "machine warmup-time" requirement with laser soldering as there is with other methods.

Along with the intended improvements in product quality, the manufacturer should be able to look forward to improved sales and profitability, to reduced field failures and warranty and other costs

and to an improved competitive position.

REFERENCES

1. A. C. Traub, "Parts Inspection by Laser-beam Heat Injection," NDT International, Vol. 21, pp. 63-69, April 1988.

2. Personal communication, Chris Fanelli, AT&T Federal Systems Division, Burlington, N.C.

3. B. Roeger and R. Morrison, "Laser Inspection System Provides Process Control Data," Electronic Packaging and Production, Vol. 27, pp. 128-129, February 1987.

4. J. P. Streeter, "Production Implementation of the Laser/INSPECT System," Proceedings of the Sixth ALIT Meeting, Schaumburg, IL, Sept. 1987.

5. W. Pettross, "Use of the Vanzetti Laser/INSPECT System for Process Control," ibid.

6. G. W. Fugate and J. R. Felty, "Automation of Solder Joint Inspection Procedures Utilizing Laser Induced Infrared," IEEE Transactions on Components, Hybrids and Manufacturing Technology, Vol. CHMT-10, pp. 374-378, Sept. 1987.

7. Editorial Staff, "Texas Instruments Boosts Reliability of Navy High-Speed Antiradiation Missile," Aviation Week & Space Technology, Vol. 124, pp. 96-98, April 7, 1986.

8. C. Lea, "A Scientific Guide to Surface Mount Technology," Electrochemical Publications, Ltd., Ayr, Scotland (1988).

9. Editorial Staff, "Intelligence Comes to Laser Soldering," Electronics, Vol. 59, pp. 75-77, July 10, 1986.

10. R. Vanzetti, "Intelligent Laser Soldering and Process Control," Proceedings of the Conference on Electronics Reliability and Measurement, pp. 85-94, NASA Langley Research Center, August 1987.

11. R. I. Alper, "Lasers Light the Way to Better PCB Solder Joints," Research & Development, Vol. 29, pp. 99-104, March 1987.

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LASER ROBOTIC WORK CELL

by

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ABSTRACT

A novel robotic soldering system has been designed that incorporates several unique features for enhancing solder joint reliability. The basic system design consists of a 50 Watt Nd/YAG laser which can be operated in either a CW or Q-switched mode, a 5-axis robot with real-time, closed-loop motion control, a 5-axis robot with real-time, closed loop motion control, a closed loop micropositioning correction system, and is controlled by an IBM AT host controller with custom menu driven software.

The Nd/YAG is delivered to the work place through an optical Q-switch by a hard lense optical path. An infrared detector monitors the temperature of the soldering process at the work location. The laser energy delivered to the work is then controlled by means of an optical Q-switch, connected to the infrared detector in a closed-loop mode. Each solder joint type has a unique temperature profile. Temperature profiles of each joint are compared to an established profile in determination of the integrity of the joint. A permanent record of each joint could be maintained through the use of the host IBM AT as a data file.

The robotic laser system is controlled at the top level by the IBM AT. The AT communicates to two Z80 controllers which in turn control the closed-loop robotic positioning and infrared monitoring system.

Preliminary results indicate solder joint reliability will be increased by several orders of magnitude when compared with hand-soldered joints. A key feature of the robotic soldering system is the inherent process control achievable with a controlled application of heat. Future applications to fine pitch packages, SMTs, and precision rework are a few of the possibilities.

INTRODUCTION

AT SBRC we produce infrared detectors packaged within vacuum dewars for the Department of Defense. A large number of solder joints (~900) are made in each dewar. The concept for using a laser to solder junctions and to cut thin metal straps was first considered in 1983 during producibility and cost savings studies. Design philosophy focused on a combination of commercial components and custom robot control mechanisms.

Work on the robotic cell started in mid-1985 and the concepts were refined during Research and Feasibility Phases. The work cell was designed and fabricated during the next several years.

The Robotic Work Station (Figure 1) is a flexible work cell, which is capable of performing various process operations using a Neodmium doped: Yttrium Aluminum Garnet (Nd:YAG) laser beam in the continuous wave or pulsed modes of operation. The Station contains the following special features: (1) an ultra-precision five-axis robot with real time, closed loop motion control, (2) infrared sensing and closed loop control of the heat zone, (3) full automation using an IBM AT host computer and custom menu-drive software, and (4) on- or off-line TV viewing of the work plane. A complete description of the Robotic Work Station is presented in the next section of this report.

General

The Robotic Work Station (Figure 2) is comprised of two free standing consoles. The console on the right is the Remote Control Unit. This unit contains the IBM AT host computer and its accessory components, as well as other monitors and controllers which allow an operator to program and control the system. The console Work Station on the left is comprised of the laser system, the five-axis robot, the optical arm and the rotary work platforms. The robot is hooded and an exhaust system vents the area of smoke and soldering residue by circulating the air once every minute.

Both consoles are equipped with rollers so they may be readily moved about to facilitate system operation in any type of location. For current operations, they are situated next to each other in the same room, and at an approximate 45 degree angle. This allows an operator sitting on a swivel chair to access one console or the other with ease. Another design feature which facilitates system operation is the open front on the Work Station; it is not only convenient for a human operator to load and remove parts, but it is also adaptable to robotic parts handling in a future mode of operation.
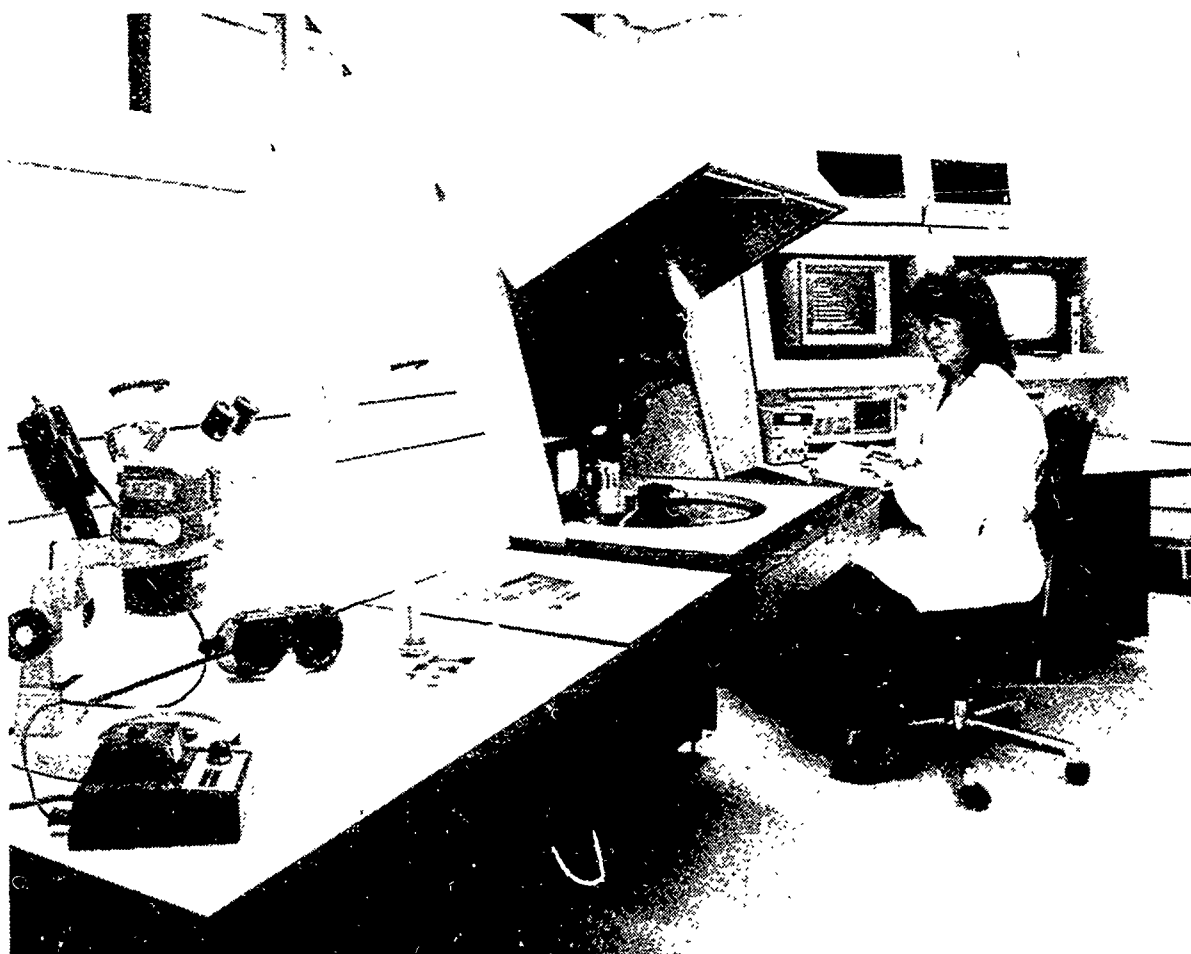
FIGURE 1. The Robotic Work Station is a Flexible Work Cell
for Performing Soldering and Strap Cutting Operations on the
Common Module Detector Dewar.

Remote Control Unit

The Remote Control Unit (Figure 3) provides the controls,
monitors and instrumentation for complete operator interaction
with the Robotic Work Station. The principal control function
is provided by the IBM AT host computer, located on the lower-
left panel of the unit. The IBM comes equipped with keyboard,
hard disk memory and, to its right, a printer that is recessed
into the table top. The computer monitor sits on the left-hand
shelf above the IBM; it will display the menu driven program for
booting up the system, or if the system is in operation, the
host routine that is currently being run at the work station. A
second monitor, to the right, is for the TV cameras; black and
white is used with the on-line camera to provide a high resolu-
tion image of the work area, color is used with the off-line
camera to display a realistic image of the entire work piece.

COVER ON AIR SHOCKS

PARTS STORAGE

POP-UP
COVER
PANEL

LASER POWER
SUPPLY

TOOLS &
STORAGE

CONTROLLER-
COLOR MONITOR

LASER / ROBOT
ARM

IBM DISK DRIVE

SWIVEL TABLES

KEYBOARD

ROBOT &
TABLE CONTROLLER

TILTABLE
MONITORS

ON-LINE &
OFF-LINE
CAMERA
MONITORS

ROBOT DRIVERS
& MOTORS

PRINTER

WORK STATION

REMOTE CONTROL
UNIT
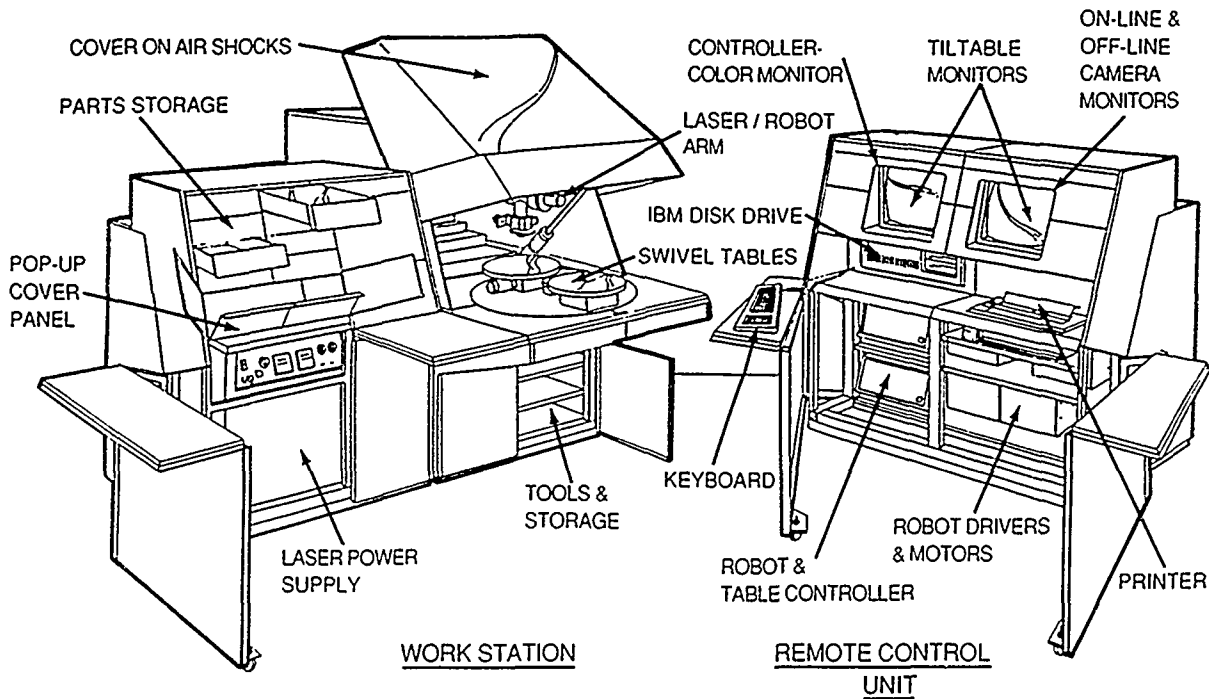
FIGURE 2. The Robotic Work Station, Comprised of Two Free
Standing Consoles, the Work Station and the Remote Control
Unit.

Two microprocessor controllers are shown sitting on top of
the monitor shelves in Figure 3. They are in this position only
for engineering programming purposes; they are normally placed
in the storage area below the table. The left-hand controller
is for the robot, the right-hand controller is for the rotary
work platforms. The controllers continuously display the exact
position of all driven axes while the system is in operation.

Laser System

The Robotic Work Station incorporates two commercial laser
systems. First, there is the Nd:YAG system, manufactured by
Control Laser Corporation. It produces radiation in the near-
infrared (1.064 nm); its continuous power capabilities (up to 50
watts) are adequate for performing all work station operations
of soldering and cutting. Second, there is the Helium Neon
(HeNe) laser system, manufactured by CR Laser, which is used as
a pointing laser. Because the 1.064 nanometer output of the YAG
is not in the visible range, the low power, red HeNe laser beam
is aligned with the optical axis of the YAG beam so its location
may be observed on the work plane.

The YAG laser system consists of two basic units: (1) the
head assembly which consists of a laser pump cavity, associated
mirrors and mounts, and an acousto-optic Q-switch, and (2) the
power station which contains a Krypton-arc-lamp power supply, an
acousto-optic RF driver and a water-to-water heat exchanger.
The laser head is completely enclosed complying with all appli-
cable safety regulations. It sits on a flat isolation table and
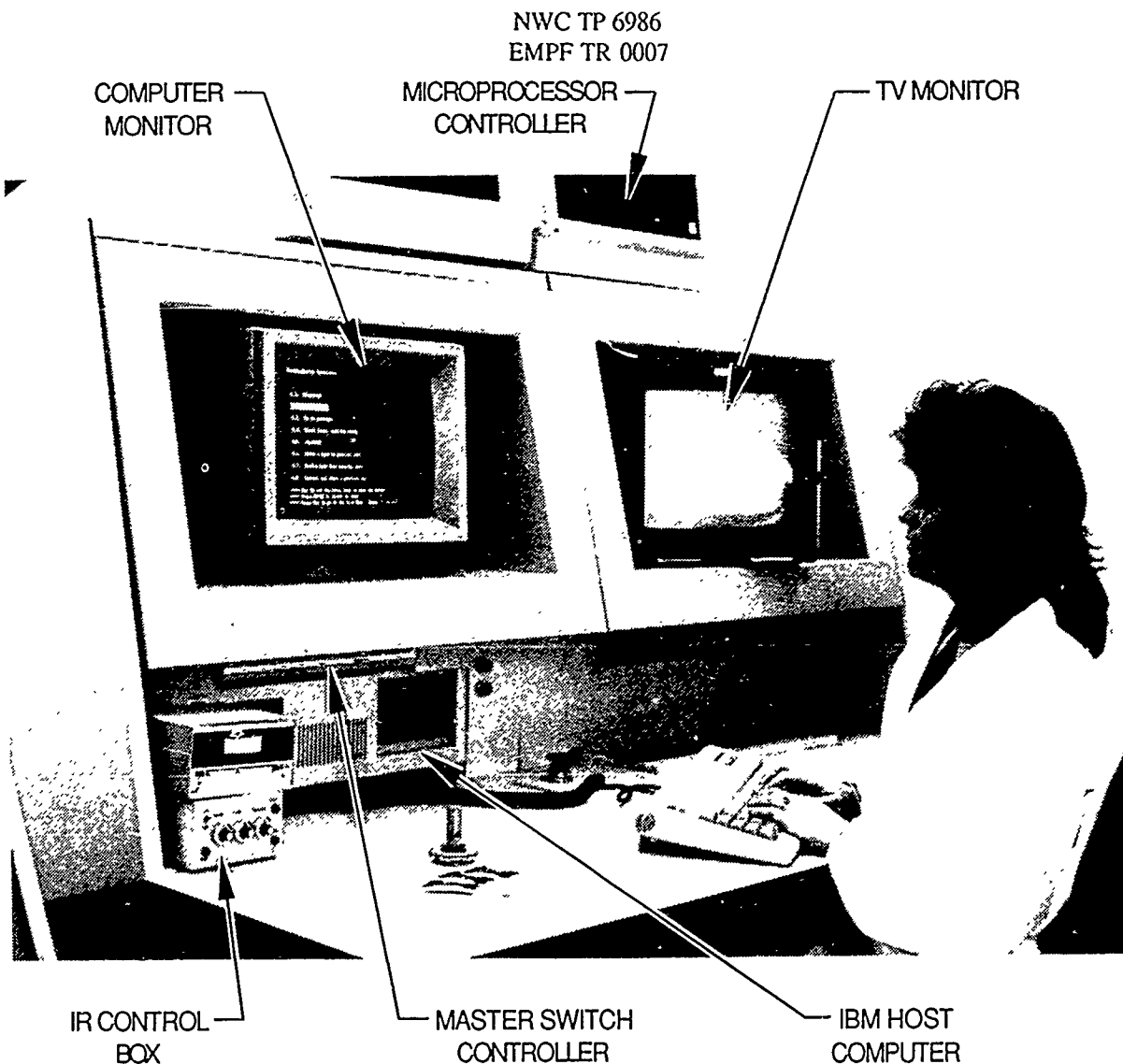
FIGURE 3. The Remote Control Unit Provides the Controls, Monitors and Instrumentation for Complete Operator Interaction with the Robotic Work Station.

aligns so the laser beam projects horizontally into the X-axis arm of the robot, which also sits on the same isolation table. The power supply is located below the laser head and accessed through a door on the lower left of the Work Station. The laser power supply is not controlled from the master switch panel on the Remote Control Unit, but must be turned on and off every time the Robotic Work Station is used. Other laser power supply controls which must be set for system operation are: (1) a toggle switch sets the Q-switch mode, and (2) the "current adjust" knob sets the maximum laser power level.

Dual Rotary Work Platforms

A large circular hole cut into the table top of the Work Station accommodates the dual rotary work platforms which hold the parts being soldered or trimmed (Figure 4). Both platforms are flush with the table top and mount on a large circular base

BASE TABLE ⟍

ROTARY WORK
PLATFORMS
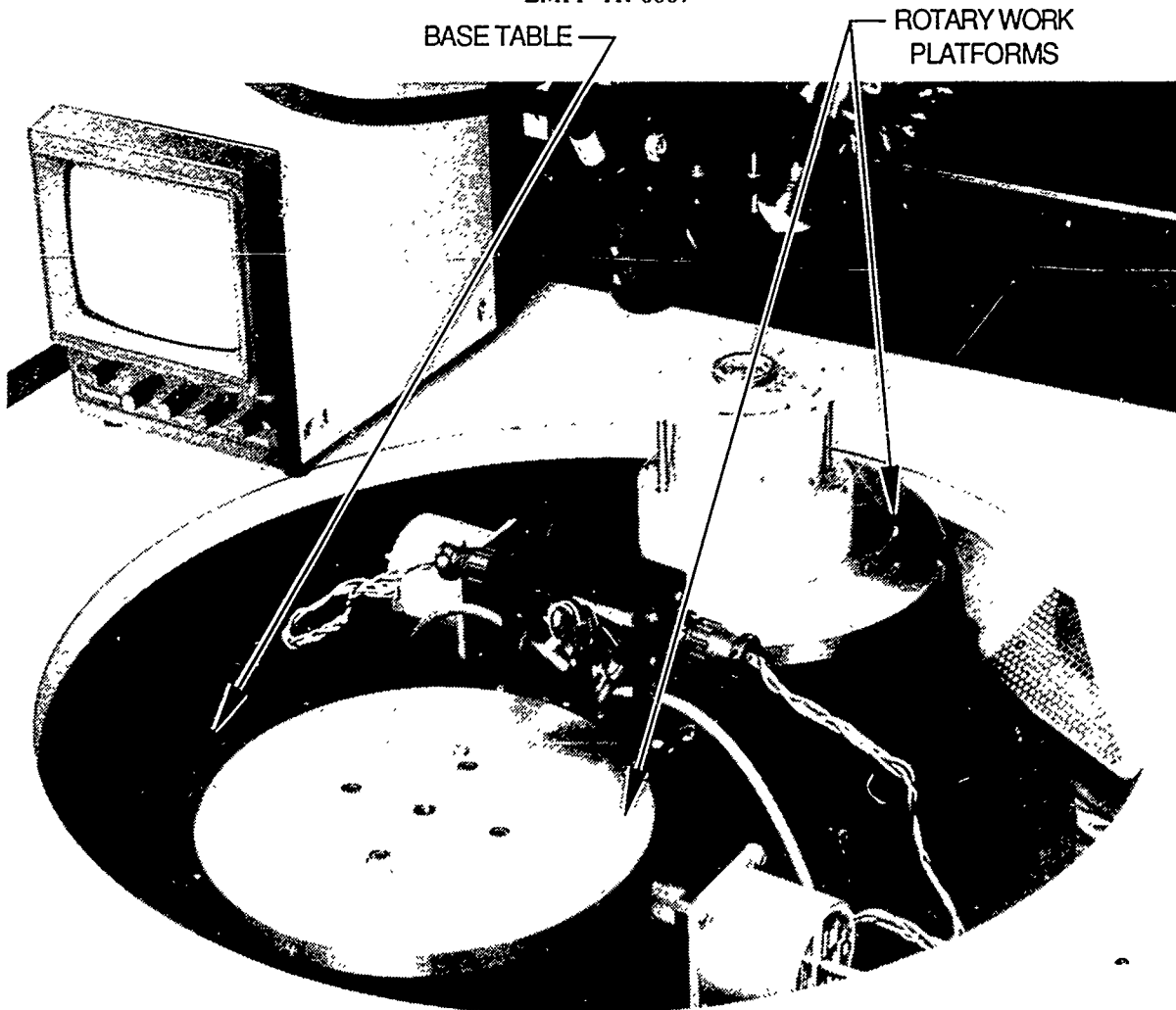
FIGURE 4. Dual Rotary Work Platforms Accommodate Parts for
Soldering and Trimming.

that is recessed into the hole. The base can rotate 180 degrees
to hard stops at either the front or rear of the table, thus
presenting one rotary platform to the operator while the other
is located under the end effector of the robot. The two rotary
platforms are identical. Each accommodates a payload of about
10 pounds, and provides 360 degrees of motion in steps of
1/100th of a degree; each is also equipped with precision pins
for tooling location. The inherent accuracy of these platforms
makes them compatible with an alignment program, which automati-
cally corrects rotational errors in the part being worked on by
calculating a rotary action and moving the platforms accord-
ingly.

Five-Axis Robot

The robot is a motor driven mechanism which has freedom of
movement in five axes. These are, with respect to the operator:
(1) left and right (X), (2) back and forth (Y), (3) up and down
(Z), (4) rotary, and (5) tilt (see Figure 5).

ROBOTIC MOTION DIAGRAM

WORKSTATION MOTION DIAGRAM
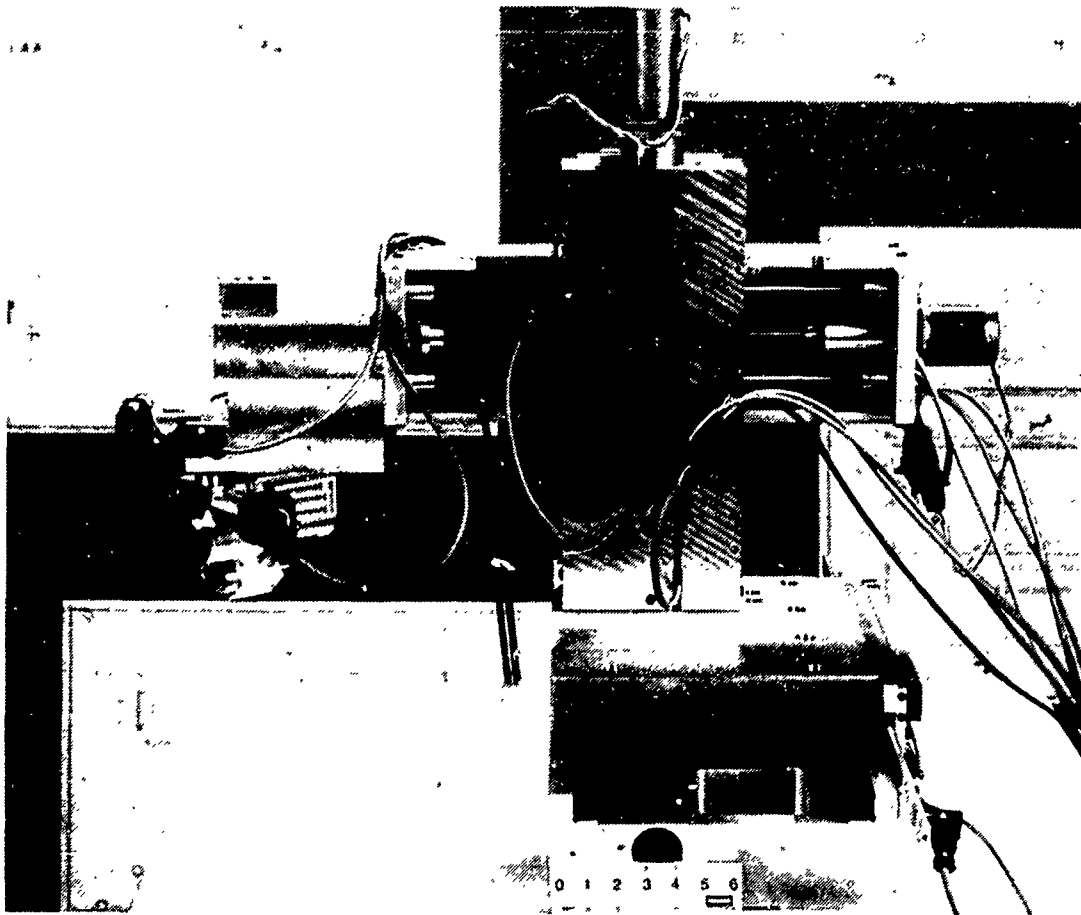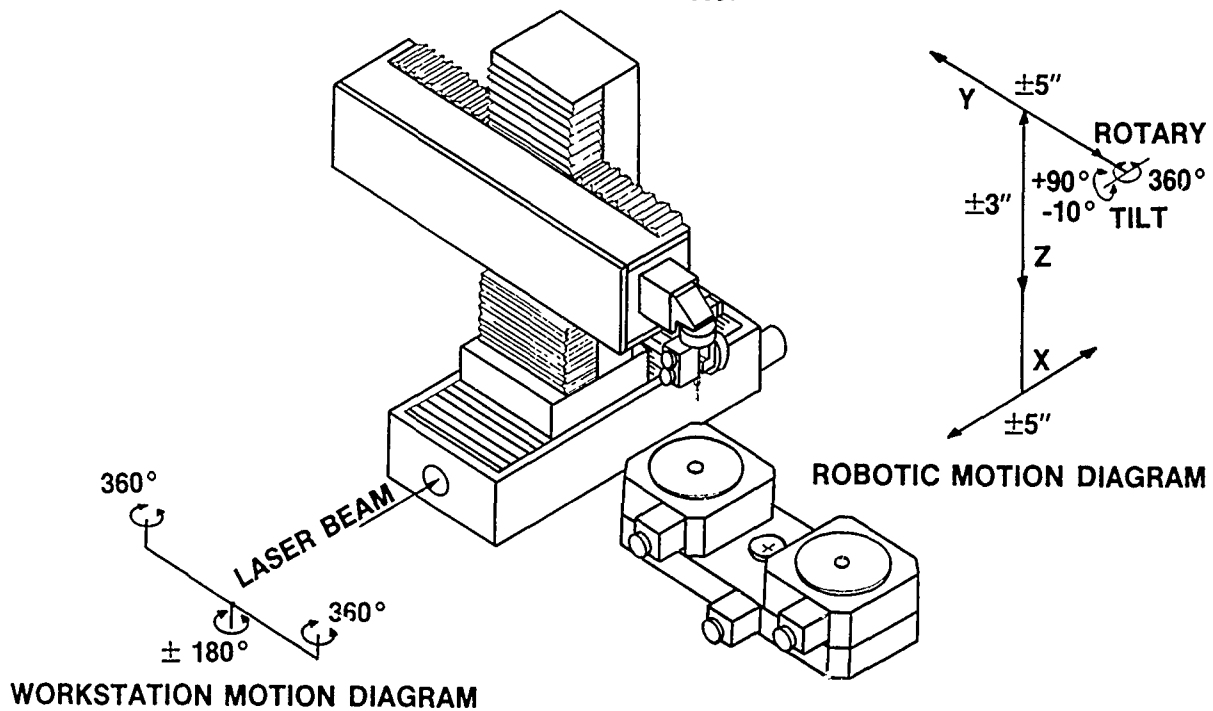
FIGURE 5. The Robot is a Motor Driven Mechanism with Freedom of Movement in Five Axes.

The robot mounts on a vibration damping table on the same plane as the laser. It is made from rough cut aluminum stock and within its hollow arms contains hard optical components for directing the path of the laser beam from the laser head to the end effector. The X arm of the robot is located at the base, the Z arm extends vertically from the X arm, and the Y arm moves up and down the Z arm. These linear axes are lead screw driven and provided with accordion-type dust covers to protect moving parts and optical areas from dirt, dust, and soldering debris. The rotary axis mounts on the front edge of the Y arm with the tilt axis mounted beneath it. The rotary and tilt axes combine to form an assembly called the rotary-tilt head (shown in Figure 6). The final focusing lens, or end effector, is situated at the bottom of the tilt head. It is a lens which provides the laser focal length to the work plane. Also mounted on the rotary-tilt head are two fiber optic lamps which illuminate the work area. The lamps move along with the end effector as the robot repositions itself for soldering from pin to pin. The lamps thus provide a constant lighting scenario which is critical for proper operation of the pin detector.

The laser path through the hollow interior of the five-axis robot is illustrated by the dashed line in Figure 7. The laser fires through a hole in the lower edge of the robot to a mirror on the X axis. The beam is deflected straight up the Z arm to another mirror which deflects the beam through the Y arm to the rotary-tilt head. Additional mirrors in the rotary-tilt head then direct the beam through the end effector to the work plane.

Optical Arm

The optical arm is mounted towards the rear of the Y-axis arm of the robot. A photo of the optical arm (with covers removed) is given in Figure 8. At the top of the figure is also a schematic of the paths taken by both infrared and visual images as they travel through the optical arm; solid lines depict visual and coincident visual/IR images and dotted lines represent IR alone.

The image from the work plane is reflected through the final focusing lens in the end effector and directed through the rotary-tilt head up to a mirror at the top of the assembly. The image is then directed 90 degrees (X axis) to a second mirror, which deflects it another 90 degrees into the Y axis. Now within the optical arm itself, the image passes through a tube to a coated filter (refer to the schematic in Figure 8). The purpose of this filter is to block out the 1.06 nm wavelength of the YAG laser so it does not flood the optics. The image is then directed to a Dichroic beam splitter, which separates the visual and the IR images. The Dichroic beam splitter transmits the IR directly through to an infrared detector, whose operation is discussed in a later section of this report. The Dichroic

TILT AXIS ———
ROTARY BEARING
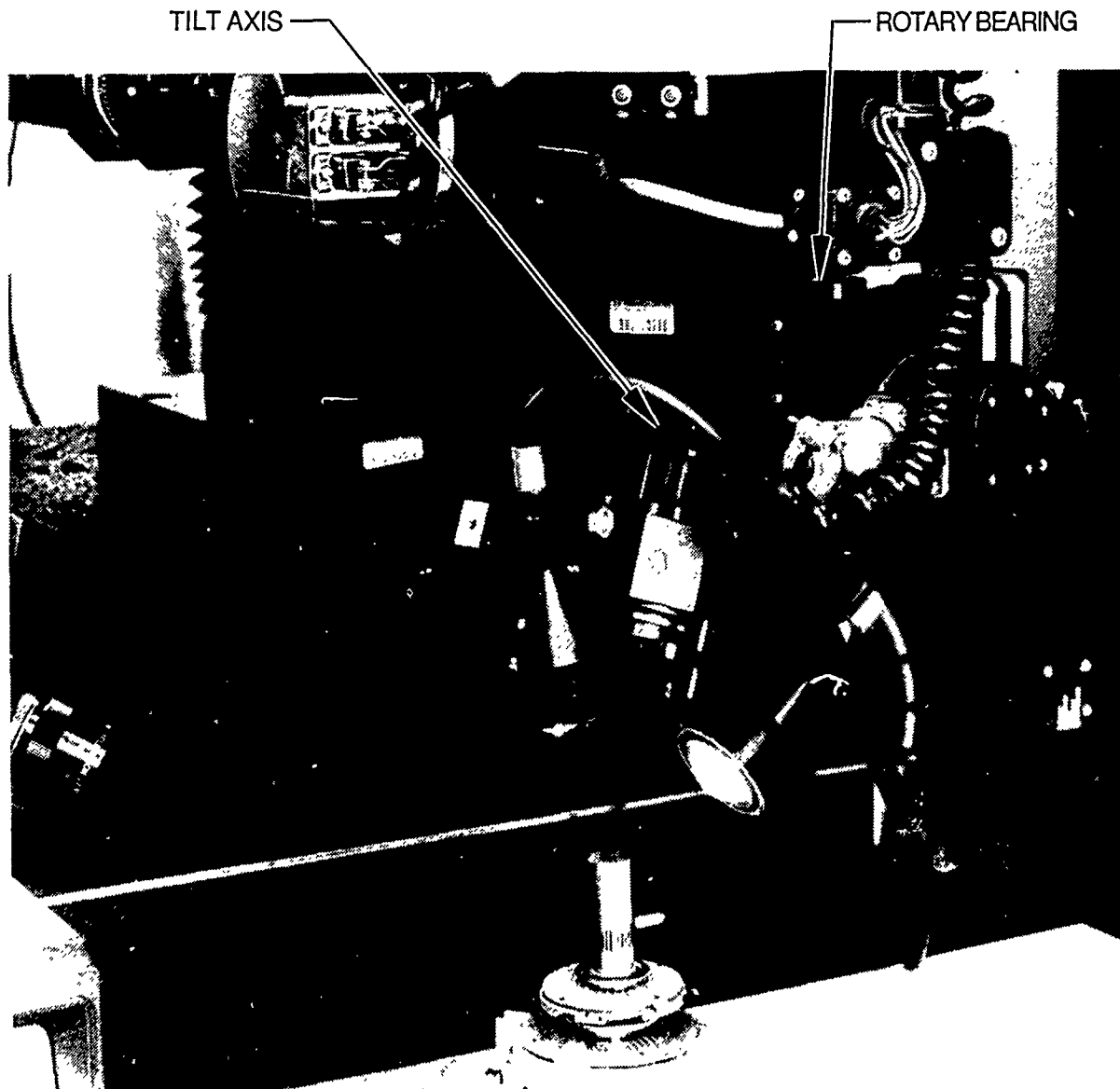
FIGURE 6. The Rotary and Tilt Axes Combine to Form the
Rotary-Tilt Head.

beam splitter also deflects the visual image down (Z axis) to a
mirror, which then deflects the image another 90 degrees along a
lower Y axis path in the optical arm. An adjustable focusing
lens in this lower path focuses the image to the field of view
of the work area (approximately thirty-thousands of an inch for
soldering), and directs the image to a visual beam splitter lo-
cated directly behind the lens. The visual beam splitter then
splits the image in two directions: (1) horizontally to the on-
line TV camera, and (2) vertically to the upper optical path
where a mirror deflects the image 90 degrees into the pin detec-
tor (whose operation is discussed in a later section of this re-
port). All components on the optical arm are on hard mounts cut
with slots so they may be moved precisely into the optical path
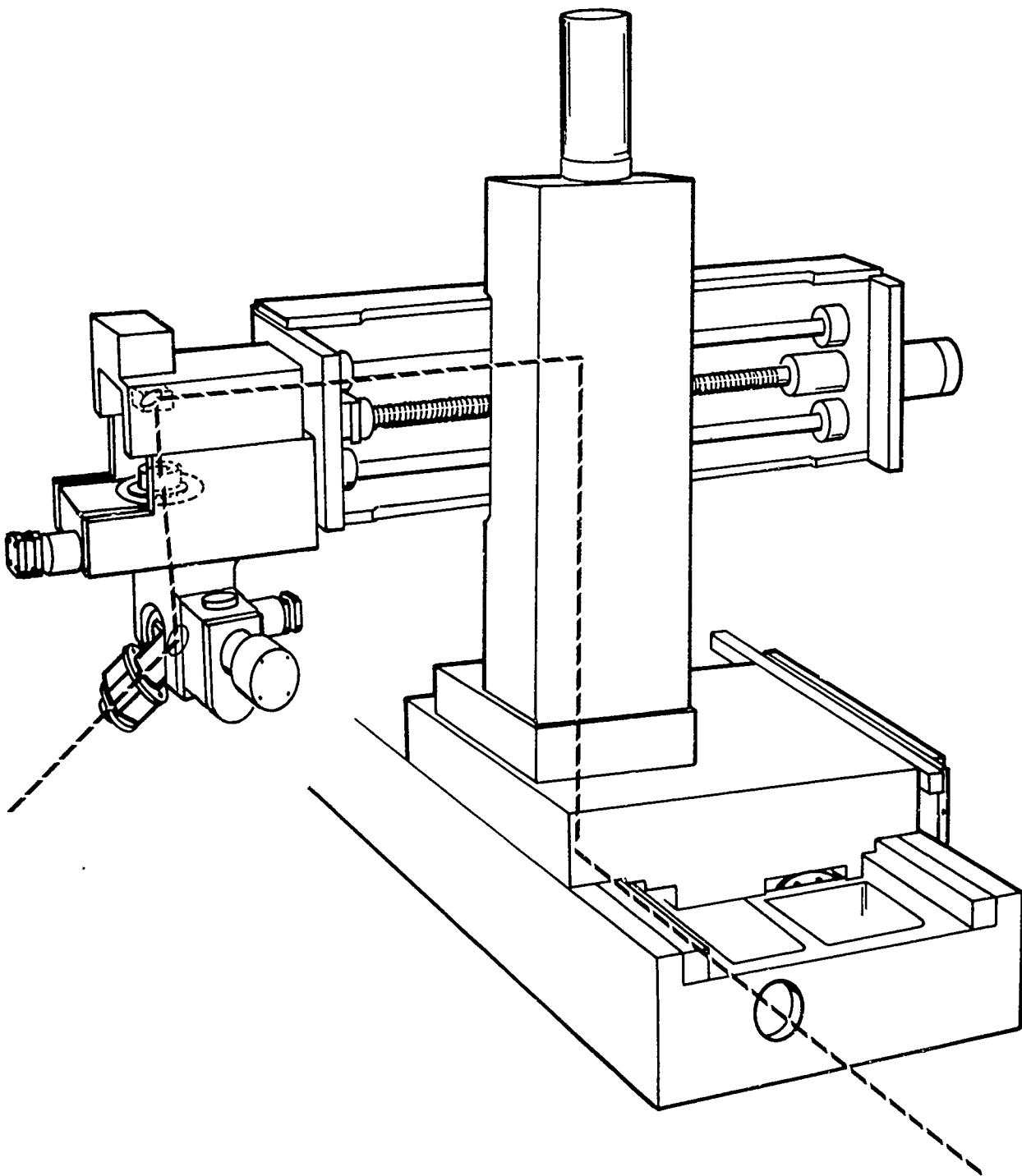
FIGURE 7.   The Laser Delivery System is Provided by Hard
Optics within the Hollow Core of the Robot.

PIN
DETECTOR

INFRA-RED
DETECTOR

DICHROIC
BEAM
SPLITTER

FILTER
LENS

MIRROR

IR IMAGE

TV
CAMERA

BEAM
SPLITTER

FOCUSING
LENS
(ADJUSTABLE)

MIRROR

IMAGE
REFLECTED
FROM
WORK
PLANE

PIN DETECTOR
MOUNT

IR DETECTOR
MOUNT

BEAM
SPLITTER

ON LINE TV
CAMERA

OFF LINE
TV CAMERA
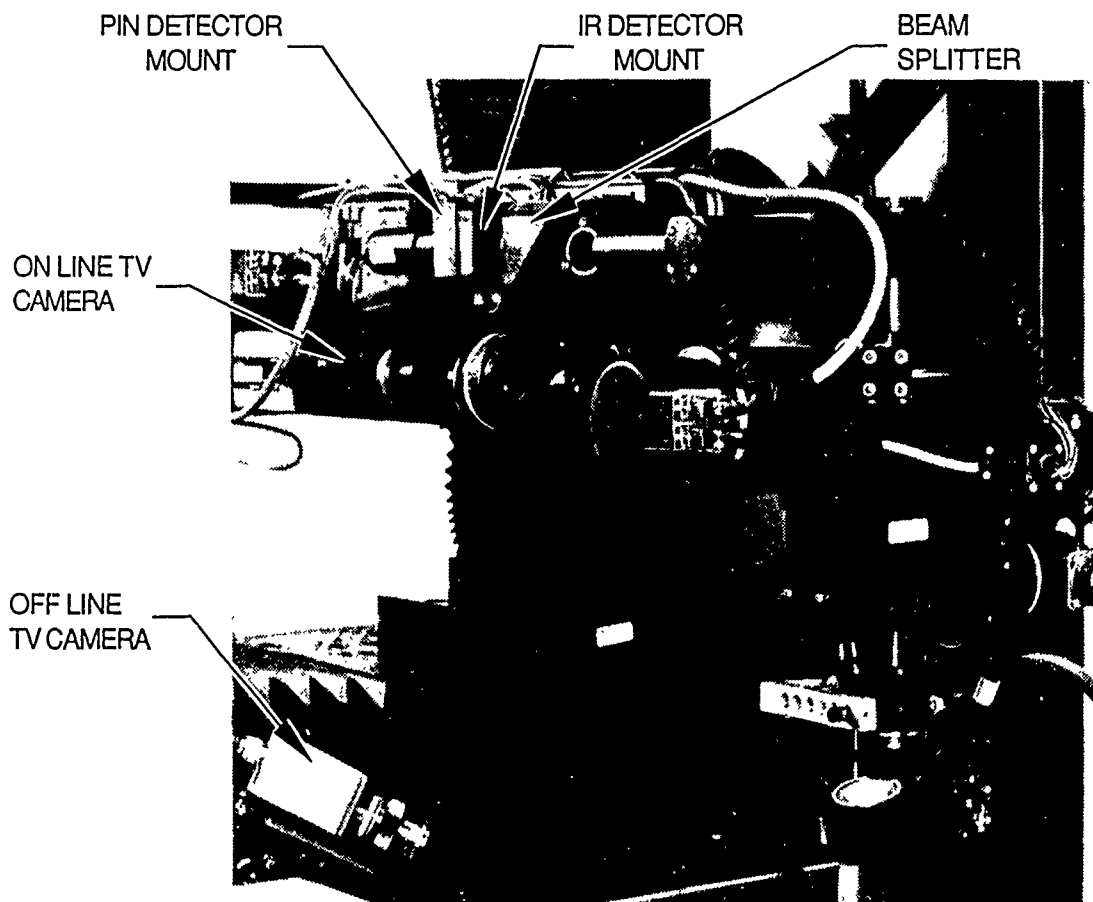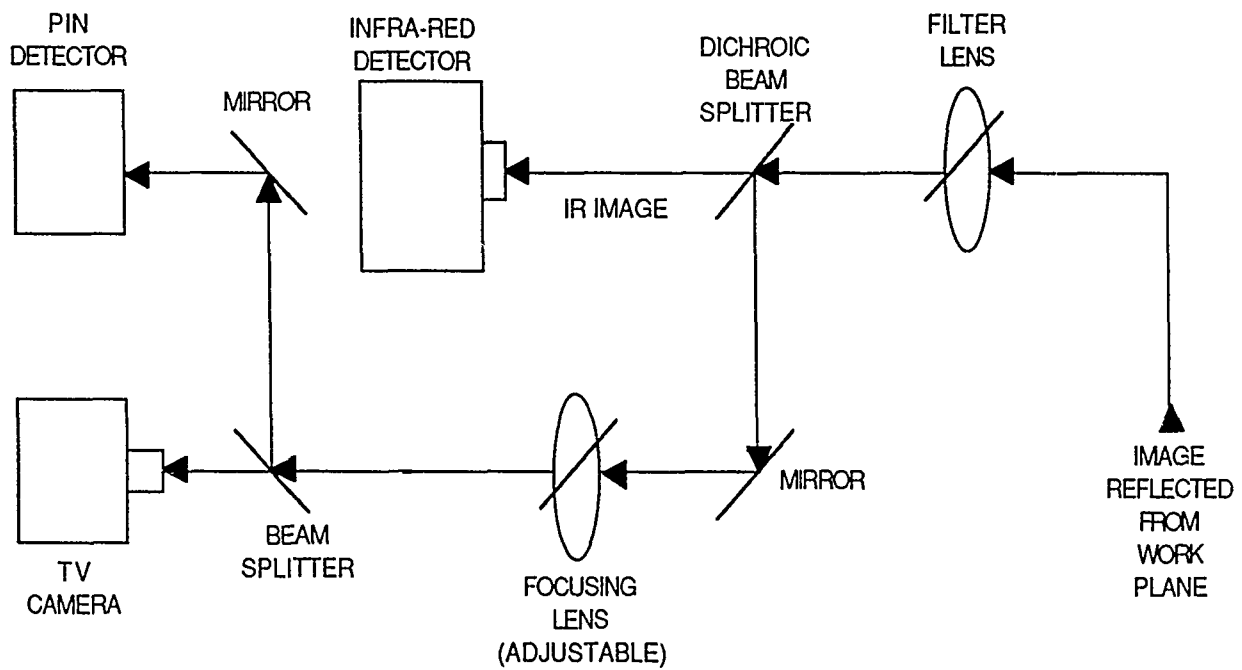
FIGURE 8. The Optical Arm Provides Separate Paths for the
Visual and Infrared Images from the Work Plane.

of the laser. The on-line alignment procedure involves the fol-
lowing steps. First, the location of the YAG beam is determined
using black laser paper. The HeNe laser is then adjusted so its
red dot shines directly over the YAG beam. The optical compo-
nents are then physically moved about until the HeNe image is
centered on the optical path of the TV camera. The on-line TV
monitor thus shows exactly where on the work plane the laser is
firing.

Real Time Motion Control System

A generic block diagram of the real time motion control
system for the robot and the rotary work platforms is presented
in Figure 9. This system comprises the IBM AT host computer
and, for each individual stage, a microprocessor controller, a
dc motor, and a positional encoder. Besides the mechanical con-
figuration of the stages themselves, the principal difference
between motion control systems lies in the positional encoders.
Heidenheim linear encoders are utilized in the X, Y and Z stages
of the robot; rotary optical encoders are utilized in the rotary
and tilt stages of the robot as well as the rotary work plat-
forms. Also, the pin detector is functional only in the track-
ing mode of the X and Y axes of the robot, as will be described
below.
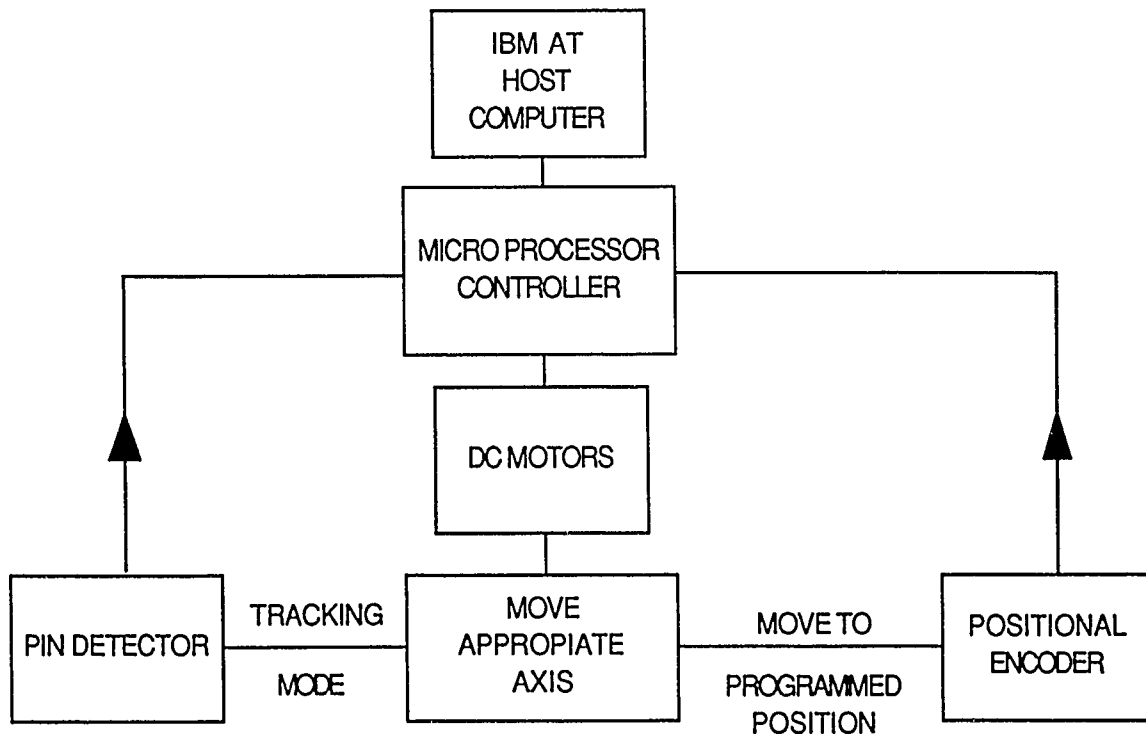
FIGURE 9. Motion Control System Provides Real Time Feedback
to Microprocessor Controllers.

Operation initiates at the host computer, which is prepro-
grammed with the data points for each axis and an outline rou-
tine for the entire process. The data points, comprising both
positional and velocity information, are first transferred to

the microprocessor controller and stored for the duration of the process. The IBM then enters into its host routine, which is an outline of when each data point is to be activated. As each data point comes up in the program, ASCII to dc encoder boards within the controller generate drive signals for the motors, which then move the appropriate axes at preset velocities toward their programmed positions.

A positional encoder continuously monitors the actual position of each stage and provides real time feedback to the microprocessor controller. By comparing the actual position with the desired one, the controller can then decide whether or not to continue driving the motor. The controller also knows how to make necessary corrections if a stage travels beyond its designated position. Once the stage is in position, the encoder continues to send real time feedback to the controller so that corrections can be made if it moves off for any reason. The microprocessor controller will send a message to the IBM informing it when all stages are properly positioned as programmed. In practice, this will mean that the laser axis is in the field of view of a pin to be soldered, that is, within .030 inches of the true center of the pin. The IBM will then activate the tracking mode, enabling the pin detector instead of the encoder to provide feedback control to the microprocessor controller.

The pin detector comprises a solid-state quadrant detector and associated electronics. The image of the pin and its surrounding area is projected onto the sensitive area of the quadrant detector. Photogenerated currents are thereby induced in each of the four active regions of the detector, causing a current to flow into the external circuit. The magnitude of the current flowing from each quadrant is proportional to the integrated light flux falling on that quadrant. The difference between signals from opposite quadrants yields a normalized transfer function specifying the position of the spot. The differential signals from the quadrant detector circuitry thus correspond to +X, -X, +Y, and -Y drive signals. These signals are coupled to the microprocessor controller, which then drives the stages to automatically center the pin in the optical axis of the robot (Figure 10).

Closed Loop Infrared Control

The key elements utilized for closed loop infrared control are the optical Q-switch, infrared detector and its controlling electronics, and the IBM AT host computer (Figure 11). The Q-switch functions like an optical gate in the laser path. When excited, it deflects a portion of the beam off the optical path; the greater the excitation voltage, the more opaque the Q-switch becomes. When it is turned off, the Q-switch becomes transparent and projects the laser beam via hard optics in the robot to the work plane. The infrared detector is a heat sensing device that monitors the heat zone on the work plane. The output voltage from the detector feeds into the controlling electronics

**ROUGH POSITIONING
(ROBOT PROGRAMMED)**　　　　　**FINE POSITIONING
(PIN DETECTOR ACTUATED)**
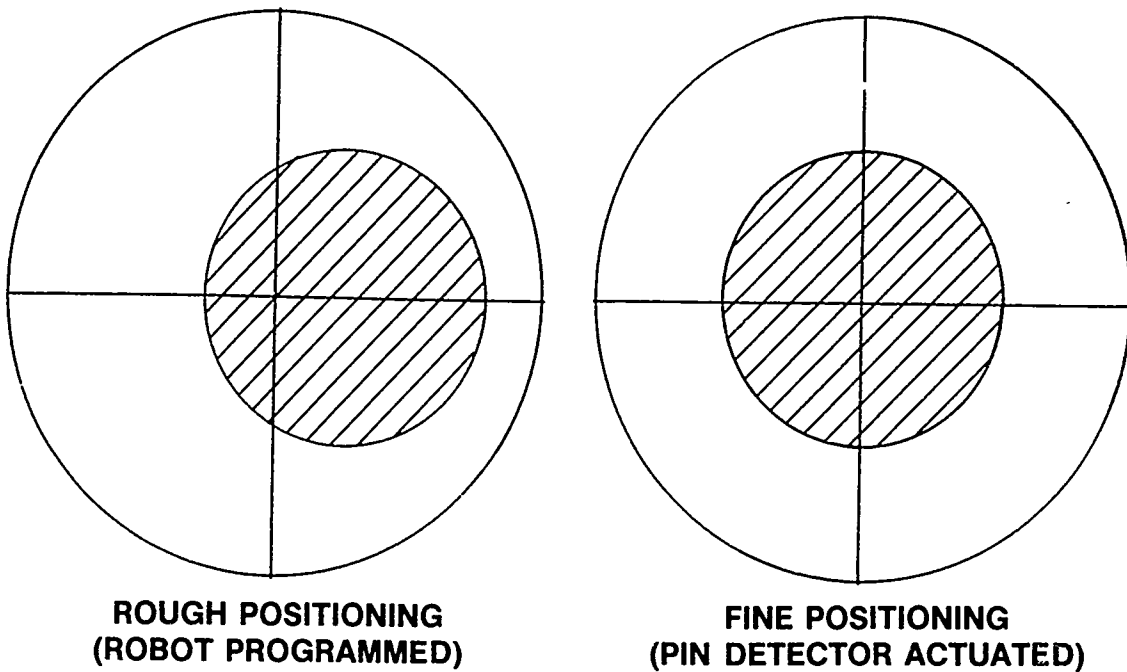
FIGURE 10. Pin Detector Fine Positions X and Y Stages to
Center Pin in Optical Axis of the Robot.
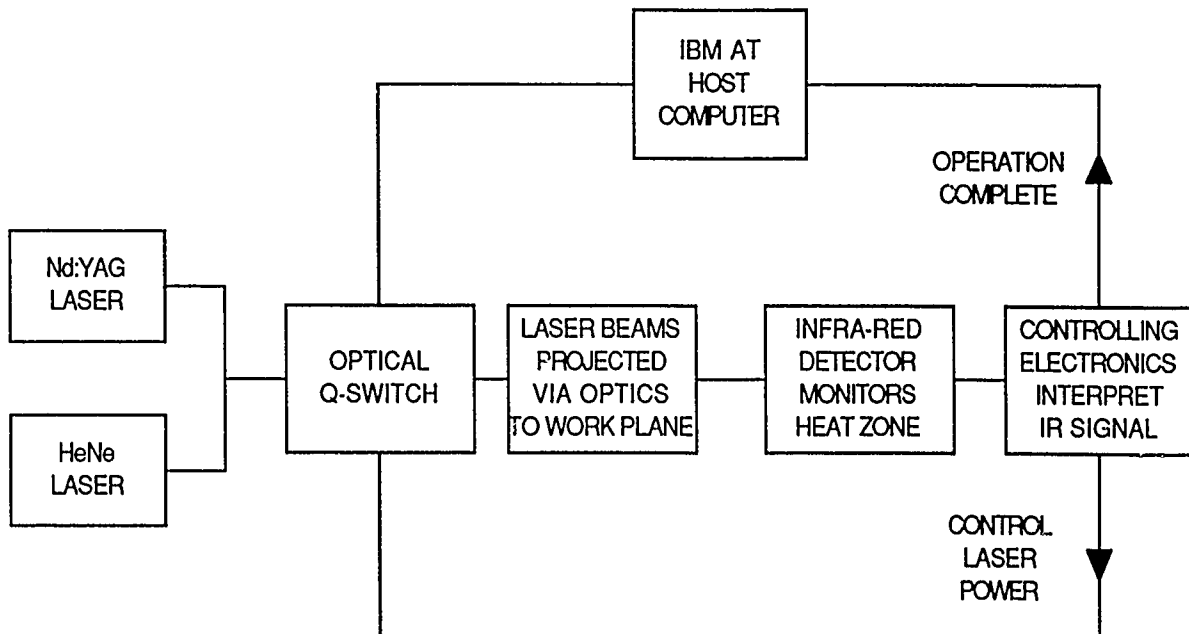
FIGURE 11. Closed Loop Infrared Control Utilizes Optical
Q-Switch to Control Laser Power.

that interprets the signal and produces an output that is lin-
early proportional to temperature. The controlling electronics
then provide feedback to the Q-switch, controlling its excita-
tion and thereby modulating the amount of laser power projected

to the heat zone. The electronics are also time settable, allowing an "operation complete" message to be generated for the IBM.

Operation of the closed loop infrared control system for a typical solder process is explained with reference to the infrared signature plot of the heat zone (Figure 12). Normally the IBM blocks the laser beam by applying +12 volts to the Q-switch. The IBM initiates soldering by turning off this voltage causing the Q-switch to become transparent. Laser power now directs to the heat zone and the temperature increases. The slope of this temperature rise is directly related to the laser power setting on the laser power supply; the higher the power setting, the faster the ramp-up. Temperature at the heat zone rises to the solder melting threshold, which is set at the controlling electronics for the infrared detector. At this point the controlling electronics feed back some excitation voltage to the Q-switch, causing it to become somewhat opaque and inhibiting laser power. Signal from the heat zone then drops rather suddenly as the solder to stabilize. A dwell period (approximately 500 ms) is now required for the solder to effectively reflow throughout the joint. During this dwell the excitation to the Q-switch is modulated by the controlling electronics, such that laser power will just maintain a constant temperature at the heat zone. At the end of the dwell the controlling electronics send an "operation complete" message to the IBM, which in turn reapplies +12 volts to the Q-switch and terminates the operation.
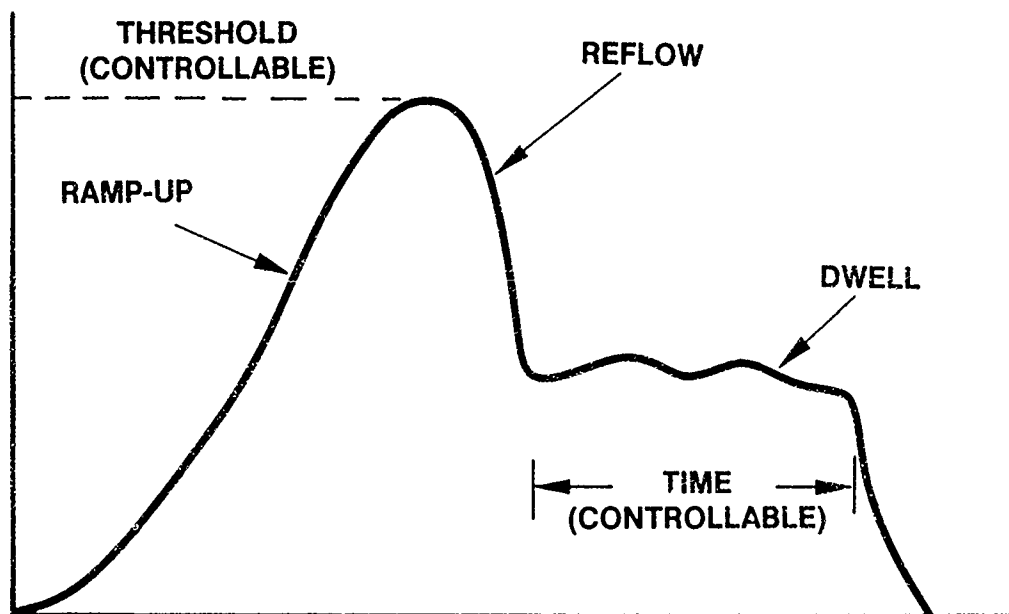
FIGURE 12. IR Signature of Heat Zone Shows Threshold and Dwell Time for Proper Soldering.

When the laser beam is used in a cutting mode, the 0 to +12 volt control signal from the IBM switches on and off at a rapid rate. Peak power in the kilowatts range can be obtained in this manner because of the optical storage capabilities of the laser rod during the beam interruption. No other type of Q-switch control is utilized during the cutting operation.

Computer Operating System

The interfaces between the IBM AT host computer system and external devices under its control is illustrated in Figure 13. Connected to the host computer is a printer, and the user interface which is a keyboard. The main controlling program, written in C, calls assembly subroutines, selected from a menu, which reside in the robotic controller. The robotic controller is the assembly code written to interface with the two microprocessor controllers. Microprocessor controller 1 drives the five-axes robot; Microprocessor controller 2, the rotary work platforms.
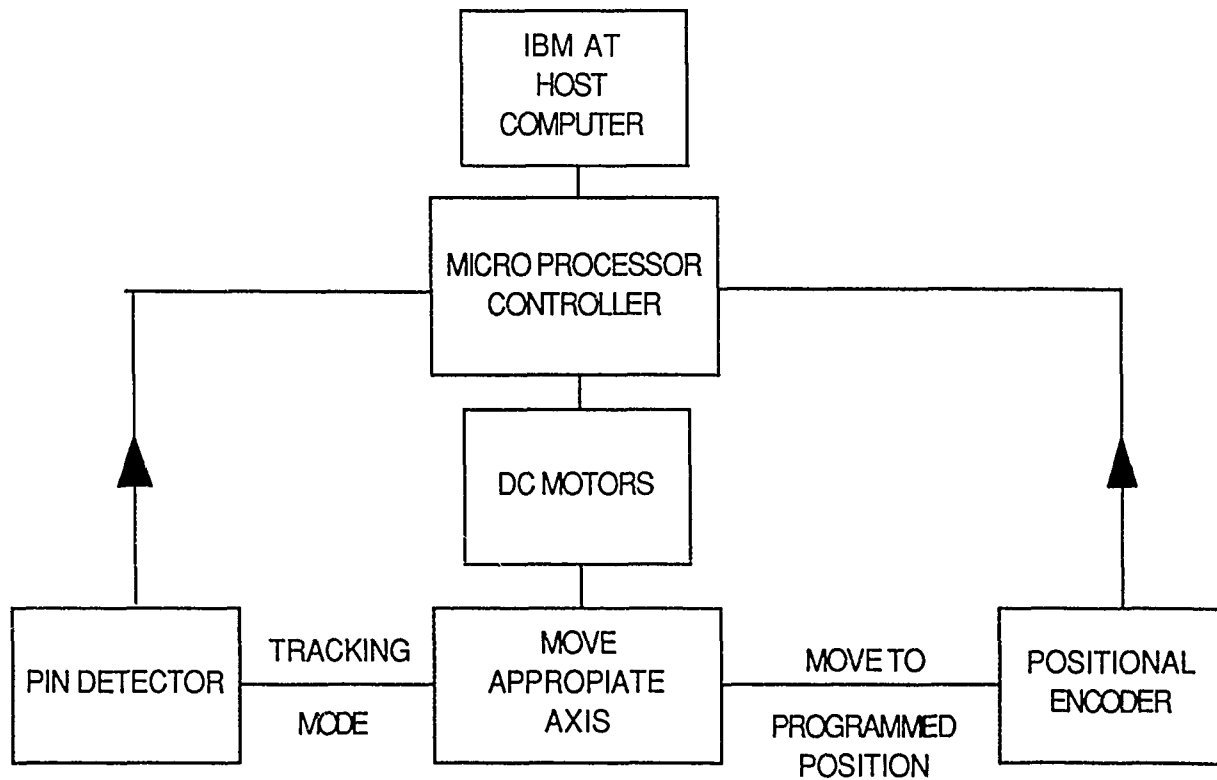
FIGURE 13. The IBT AT Host computer System Utilizes LEV25 Main Controlling Program for the Robotic Soldering Laser and the Rotary Table.

SUMMARY

A laser robotic work cell has been built which has some unique design features. This machine is currently installed in our Product Development Center and has been undergoing continuing evaluation of applicability. A follow-on effort has been initiated in connection with an Industrial Modernization Improvement Program which should result in a production device.

Finally, some areas for future activity will include:

- A continued study of solder joint thermal signatures as measured by the infrared detector

- Total closed loop control of the solder joint

- Alternate applications of the solder

- Refinement of process controls

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LESSONS LEARNED FROM INDUSTRIAL EXPERIMENTS

by

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ABSTRACT

When an experimental program is designed in an industrial environment, the primary goal is to reach a better understanding of the system, thereby providing direction toward improvement. However, in many cases the results realized are not the results anticipated and the experiment is deemed a failure. This conclusion fails to recognize, though, the fact that valuable information can often be obtained from these experiments.

This paper will describe experiments that were determined to be failures, yet resulted in useful knowledge being gained. It also details precautions to take when designing and implementing experiments. Most importantly, it describes ways to analyze the responses received in experiments and to capitalize on unexpected results. In this way, we can determine the lessons that can be learned even in failed experiments.

INTRODUCTION

In the effort to improve manufacturing processes, engineers use various approaches. Many use Statistical Process Control (SPC) techniques which make use of data collected during actual production. The purpose of SPC is to provide information concerning whether or not the process is in control. If a problem is detected, a search is conducted to find and remove the source.

Other engineers use off-line methods for process improvement. In other words, normal production is stopped in order to conduct a series of formal experiments. In this way information concerning the process can be obtained quickly, and drastic improvements can be made in a short period of time.

If a formal program of experimentation is selected, the experiments are usually carefully planned to allow the engineer to obtain a maximum of information with a minimum of stopped production time. We all hope that our experiments will run as smoothly as the examples presented in many textbooks, but in real life many things

can, and do, go wrong. It should be recognized that a great deal of valuable information can often be obtained from such experiments. This paper presents several examples of how experiments which many would consider to have failed provided useful information.

EXPERIMENTAL DESIGN AND ANALYSIS

The purpose of an experimental program in an industrial environment is to better understand the manufacturing system in order to ultimately improve the system. The engineer usually wishes to determine how some dependent variable or response is affected by changes in the independent variables or parameters. The classical method of experimentation is to vary one parameter at a time and study the effect on the response. However, many times the effect of changes in a certain parameter on the response depends upon the settings of the other parameters included in the study. For example, in testing involving a batch vapor degreaser, it was determined that a change in the boil dwell time greatly affected the cleanliness level of a printed circuit assembly when the rinse dwell time was short. However, it did not have much affect when the rinse dwell time was increased. This type of result is known as an interaction, and would not be discovered if the classical method of experimentation had been followed.

An alternative to using the classical method to study the manufacturing process is to vary more than one parameter at a time. Formal experimental designs have been developed for this purpose. The design selected for the experiment depends upon the objective of the experiment, and the number of parameters to be studied, and prior knowledge of the effects of the parameters on the response.

In cases where there are relatively few parameters to be included in the experiment and it is expected that the effect of each of the parameters on the response will be linear, a full factorial design is often selected. In this type of design, two levels are selected for each parameter and are usually coded with a + (or 1) for the high level and a - (or -1) for the low level. Every combination of these levels is then included in the design. The result of the analysis includes a determination of which parameters significantly affect the response and the magnitude of the effect. In addition, the effects of interactions can also be calculated.

When there are a large number of parameters to be included in the experiment and the purpose of the test is to determine which parameters significantly affect the response, some type of screening design is usually selected. Again, two levels are selected for each parameter. The runs to be included in the design are usually a fraction of those included in a full factorial design. The result of the analysis of the experiment includes a determination of which parameters significantly affect the response, and whether a change in each of the parameters has a positive or negative effect on the response. A screening design is often the first step in an experimental program. Once the independent variables which have the greatest effect on the response have been designed, these are included in a full factorial design or the type of design described next, the response surface design.

If there are relatively few parameters to be included in the experiment and the effect of the parameters on the response is expected to be nonlinear, a response surface design is usually selected. Three levels are commonly used for each parameter, and are coded with a -1 for the low level, a 0 for the center level, and a 1 for the high level. The number of runs included in the design is slightly larger than that of a full two-level factorial design; however, not all combinations of parameter levels are run. The result of the analysis of this type of design include a determination of which parameters significantly affect the response, the magnitude of the effect, and an estimate of the amount of curvature associated with the effect. In addition, contour plots are often created to illustrate how the response changes over the experimental region.

The type of analysis used in order to determine whether or not the change in a certain parameter affects the response is known as a statistical test of significance. The population is the total number of measurements made of the response under similar conditions. For manufacturing processes this is usually assumed to be infinite since measurements can be made indefinitely into the future. The sample size is the number of runs in the experiment made at a certain parameter level. The test of significance is attempting to determine whether or not the samples are significantly different (in other words, whether or not they could have come from different populations). The final conclusion from this type of analysis is usually a statement such as "we are 95% confident that a change in the boil dwell time significantly affects the cleanliness level of the EMPF standard board". The level of significance is selected by the engineer; several of the values used in the calculations are dependent upon the desired significance level.

DESIGN PRECAUTIONS

Clearly Define the Experimental Objectives

The first step in a program of experimentation is designing the experiment itself. In the process of designing the experiment, certain precautions should be taken to ensure that the results will meet the objectives of the program. In order to accomplish this, the objectives of the experiment must be clearly defined.

Determine the Accuracy of the Response

Another precaution relates to the measurement of the response. The result of any analysis is only accurate to within the accuracy of the response measurement device. On several occasions, experiments have been conducted, only to discover that there was so much error attributable to the measurement technique that no clear conclusions could be reached.

For example, a screening design was conducted to determine which parameters on one of the wave soldering machines significantly affected the number of defects. Analysis of the experiment indicated that none of the machine parameters significantly affected the response. The engineer knew that changes in the machine parameters should affect soldering quality; therefore, further analysis was conducted in order to

determine the validity of using visual inspection results as a measure of quality. Each board was inspected by two inspectors and a correlation coefficient (R) was computed in order to determine the strength of the correlation between inspectors. It was determined that there was too much variability between inspectors so the responses varied widely. Hence, no accurate conclusions could be made. It was also determined that several of the defect types used to measure soldering quality had relatively low correlation coefficients, indicating that the use of this response as a measure of quality is extremely subjective and therefore not repeatable.

Select Feasible Operating Regions for Each of the Parameters

A third precaution relates to the selection of the levels of the independent variable to be included in the experiment. The range should be wide enough to detect differences in the response between levels. The levels selected should also be within the practical operating region. Finally, the engineer should make certain that every combination of parameter levels to be included in the design is feasible.

This was the problem with one of the experiments conducted using the batch vapor degreaser. A two-level factorial design was used in order to determine the effect of varying the parameters associated with the machine on the cleanliness level of the EMPF standard board. (In this experiment the independent variables were boil dwell time, vapor dwell time, rinse dwell time, and vapor spray dwell time.) The initial experiment indicated that changing the levels of the independent variables did not significantly affect the response. Examination of the levels included in the experiment led to the conclusion that the lowest level selected for each variable was probably long enough to adequately clean the boards assembled in the facility. A second experiment was conducted which included lower levels for the parameters under test. The results pointed to the boil dwell time (and possibly the rinse dwell time) as the factor which significantly affects the cleanliness level of the EMPF standard board.

Randomize the Experiment

A fourth precaution to follow is making certain that the order of the experimental runs is randomized, and the units to be included in the experiment are selected randomly. There are many reasons for randomization. The first is to minimize the effect of systematic sources of variability, such as operator fatigue or differences between lots. Randomization is the method for dealing with these unavoidable (and many times unknown) sources of variability in the results.

The second reason for randomization is to ensure that the results obtained from the statistical tests used for the analysis are valid. In *Statistics for Experimenters: An Introduction to Design, Data Analysis, and Model Building*, Box, Hunter, and Hunter write about an experiment which was conducted in order to illustrate this point. For this experiment, two populations of data were created which contained identical elements. A sample of ten was drawn from each one. Next, two types of statistical tests were used to determine whether or not the samples were significantly different. This process was repeated 1000 times. If the samples were selected from different and not identical populations, we would expect to obtain the following statement as a result of the analysis: "we are 95% confident that the two populations are significantly different".

Since the populations are identical, the test should indicate a significant difference between the samples about 5% of the time (i.e., the test would give an incorrect result). Only the data which had been collected randomly obtained the expected result approximately 5% of the time. In other words, if we are saying that we are 95% confident that the result of our analysis is correct, we should make certain that the method of data collection and the analysis technique selected allows this statement to be true.

Another experiment conducted in the facility illustrates the importance of randomization. This experiment also involved the effect of varying parameters on the batch vapor degreaser on the cleanliness level of a printed circuit assembly. As a result of the analysis, an equation was generated to allow the prediction of the cleanliness level given the machine parameters. A plot of the residuals (the observed values minus the predicted values) versus time indicated the presence of systematic variation due to an unknown cause. Further analysis pointed to changes in the flux specific gravity during the soldering process as the source of the variation. If this experiment had not been randomized, it is possible that the changes in the flux specific gravity during the test period may have varied with the changes in one of machine parameters. This would have falsely led to the conclusion that changes in this parameter affect the cleanliness level of the assembly.

USING THE RESULTS OBTAINED FROM A FAILED EXPERIMENT

Sometimes, although precautions are taken, an experiment will fail. Usually this means that the results expected are not obtained. However, valid information can be extracted from most experiments, as the following examples indicate.

The problem which is probably the most difficult to overcome is determining how to use the results from experiments which had unclear objectives. Many times, the best use of data obtained from this type of experiment is as preliminary information in the design of a new test. Any prior information concerning how the system responds to changes in parameters can be incorporated in the planning of future experiments.

When it is discovered during a program of experimentation that the response of interest cannot be measured effectively, this information can be used to refine the measurement of the response. For example, it was discovered during the analysis of the screening design run using the wave soldering machine that the use of visual inspection as a measure of soldering quality was questionable. This information was used to develop an experiment to measure the repeatability of visual inspection results. The results from this test could be used to improve the training of the inspectors involved in the visual inspection process.

Results can also be different than anticipated when the wrong levels of the independent variables are included in the experiment. For example, it was mentioned earlier that an experiment which was conducted using the batch vapor degreaser indicated that none of the machine variables specified significantly affected the cleanliness level of the assembly. In this case, further experimentation was done using shorter dwell times than were included originally, and it was determined that several of

the variables under test did significantly affect the cleanliness level. It is also useful to know that there was no significant difference in cleanliness between the levels included in the original test. If the facility were actively involved in the production of boards, this test would have indicated that shorter dwell times could be used to clean the PWBs as effectively as using longer dwell times. For a production facility, this would mean higher throughput rates and an associated savings in cost.

Finally, if analysis of an experiment indicates that variables which were not originally included in the test may have affected the response, further analysis can be done in order to determine the link between the uncontrolled variable and the response. For example, in the experiment which measured the cleanliness of a printed circuit assembly cleaned using the batch vapor degreaser, a link was found between the flux specific gravity on the wave soldering machine and the cleanliness level. This information was used in order to set up an experiment which tested the effect of changes in flux specific gravity on the response. It was determined that the flux specific gravity only had an effect when the boil dwell time was at the lowest level. Further study could be done in order to determine whether or not there is a direct link between flux specific gravity levels and cleanliness levels, or if another factor which is closely correlated with the change in flux specific gravity was affecting the cleanliness of the assemblies.

CONCLUSIONS

In spite of our precautions, experiments do sometimes fail. When this occurs, the engineer must use all of his or her knowledge of the system under test in order to make effective use of the results. Too often, the following scenario explained by Box and Draper in *Experimental Model Building and Response Surfaces* occurs.

> We have sometimes been dismayed to find that the engineer newly introduced to statistical methods may put statistics and engineering in different compartments of his mind and feel that when he is doing statistics, he no longer needs to be an engineer. This is of course not so. All his engineering knowledge, hunches, and cunning concerning such matters as choice of variables and transformation of variables must still be employed in conjunction with statistical design and analysis. Statistical methods used with good engineering know-how make a powerful combination, but poor engineering combined with mechanical and unimaginative use of inadequately understood statistical methods could be disastrous.

Only through the union of statistics and engineering can results be obtained which are effective in understanding and improving the system under test.

BIBLIOGRAPHY

Box, George E.P., Norman R. Draper, *Empirical Model Building and Response Surfaces*, John Wiley and Sons, Inc., 1987.

Box, George E.P., William G. Hunter, J. Stuart Hunter, *Statistics for Experimenters: An Introduction to Design, Data Analysis, and Model Building*, John Wiley and Sons, Inc.

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AD HOC EPA/DOD/IPC SOLVENTS WORKING GROUP: CFC EMPF TEST RESULTS

by

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ABSTRACT

Chlorofluorocarbons (CFCs) have been used widely in the electronics industry throughout the years, but have come under tremendous scrutiny lately as the prime culprit in stratospheric ozone depletion. As part of an effort to reverse this trend, this paper discusses some of the science behind ozone depletion and explains the Montreal Protocol regarding CFCs. A joint Environmental Protection Agency (EPA), Department of Defense (DOD), and the Institute for Interconnecting and Packaging Electronic Circuits (IPC) research project is also discussed. This project is designed to characterize the cleaning performance of existing CFCs and to evaluate some of the substitutes and alternatives to CFC-113.

INTRODUCTION

CFCs have been used, from refrigeration to the cleaning of metal parts and assemblies, in the electronics industry for many years. CFC-113 and its azeotropes/ blends have been the solvent of choice because of their stability, relatively low toxicity, and their ability to remove contamination with little or no post cleaning residue desposition. Although eight chemicals are controlled by the Montreal Protocol, CFC-113 is the chemical that has the greatest impact on the electronics industry. CFC-113 is used primarily to clean metal parts and circuit card assemblies. Table 1 shows the production and domestic use of all CFCs.

TABLE 1. TOTAL PRODUCTION AND DOMESTIC USES OF CFCs (1986) (MILLIONS OF POUNDS).

Application	CFC-113	Percent of Total Use
Defluxing	52.5	35
Precision Cleaning	37.5 - 45	25 - 30
Degreasing	22.5 - 30	15 - 20
Other	22.5	15
Total	150	100

SOURCE

Allied-Signal, 1988. *Recovery, Recycling, and Reuse of Chlorofluorocarbon 113.* Presentation by Joel E. Rodgers, Allied-Signal, Inc., at Process Technology '88 Conference, Sacramento, CA, 15-18 August 1988

Recent scientific studies have shown decreases in the amount of stratospheric ozone, prompting the Ozone Trends Panel to state the following in their Executive Summary.

> *While the column ozone depletion is largest in the Antarctic springtime, ozone appears to have decreased since 1979 by 5% or more at all latitudes south of 60 degrees throughout the year...The weight of evidence strongly indicates that man-made chlorine species are primarily responsible for the observed decrease in ozone within the polar vortex.* (Reference 1)

The ozone layer protects the earth from ultraviolet radiation. The chemical reactions that illustrate how a CFC molecule can destroy ozone are shown in Figure 1.

From this drawing, it is clear to see the relationship between increases in chlorine monoxide and the corresponding decreases in ozone level. Concentration of future chlorine (Cl_x) is expressed instead of ozone levels in many charts.

How Ozone is Destroyed

Ultraviolet light

Chlorofluorocarbon molecule

Chlorine atom

Ozone molecule

Chlorine monoxide

Free oxygen atom

Oxygen molecule

In the upper atmosphere ultraviolet light breads off a chlorine atom from a chlorofluorocarbon molecule.

The chlorine attacks an ozone molecule breaking it apart. An ordinary oxygen molecule and a molecule of chlorine monoxide are formed.

A free oxygen atom breaks up the chlorine monoxide. The chlorine is free to repeat the process.

FIGURE 1. CHEMICAL BREAKDOWN OF OZONE.

It is estimated that for each 1% depletion in the ozone layer there would be an increased exposure to ultraviolet radiation by 1.5 to 2.0%. According to the EPA, the global impact of ozone depletion will be observed by several changes (Reference 2). Some of these changes are listed below.

a. Increases in skin cancers
b. Suppression of the human immune response system
c. Increase in cataracts
d. Damage to crops
e. Damage to aquatic organisms
f. Increases in ground level ozone (smog)
g. Increased global warming

Table 2 shows the atmospheric lifetime and the ozone depletion potential for some CFCs and halons. Figure 2 shows how ozone levels will vary with the various controls. The ozone depletion potential is a weighing factor that relates the theoretical potential of each material to destroy ozone molecules in the stratosphere (Table 2). This potential was significant enough for the EPA to assert the following.

Because of long atmospheric residence times and transport delays to the stratosphere, stratospheric chlorine levels will continue to grow for about six to eight years even if emissions were totally eliminated. (Reference 3)

Ozone depletion potential is a critical concern. Simulations predicting the decreases in ozone levels even with model compliance to Montreal Protocol requirements indicate that the ozone level will continue to decrease for at least one hundred years. Additional controls on all ozone depleting chlorine compounds may be necessary to stabilize ozone levels. EPA expressly does not view shifting from CFC-113 to other chlorinated solvents, which are currently under regulatory scrutiny, as an acceptable solution to protecting the ozone layer. (Reference 4)

The EPA has some grim predictions regarding the ozone layer in their report of *Future Concentrations of Stratospheric Chlorine and Bromine.* Even if full compliance with the Montreal Protocol is managed by all signatories, the chlorine level will grow by a factor of 3 to over 8 parts per billion volume (ppbv) by the year 2075. This growth factor assumes continued growth of methyl chloroform, commonly known as 1,1,1 trichloro-ethane. Even if methyl chloroform emissions abruptly ceased, chlorine levels would still grow to over 6 ppbv by 2075, assuming full compliance with the Montreal Protocol. Only by reducing all fully halogenated compounds and imposing a freeze on methyl chloroform use could this trend be arrested. By such an action, chlorine and halon presence in the atmosphere would be stabilized at current levels (around 2.7 ppbv) during the next 100 years. (Reference 3)

TABLE 2. ATMOSPHERIC LIFETIME AND THE OZONE DEPLETION POTENTIAL.

Compound	Ozone Depletion Potential	Atmospheric Lifetime (years)	Amount used U.S. (millions of kg)	World (millions of kg)	Major Uses	Regulated by Protocol
CFC-11	1.0	64	79.7	368.3	rigid and flexible foams, refrigeration	yes
CFC-12	1.0	108	136.9	455.0	air conditioning, refrigeration rigid foam	yes
CFC-113	0.8	88	68.5	177.0	solvent	yes
Halon 1211	3.0	25	2.8	7.1	portable fire extinguishers	yes
Halon 1301	10.0	110	3.5	7.0	total flooding fire ext. systems	yes
Halon 2402	6.0	*	*	*		yes
Methyl Chloroform CH_3Cl_3	0.15	*	*	*	solvent	no

* = Not available
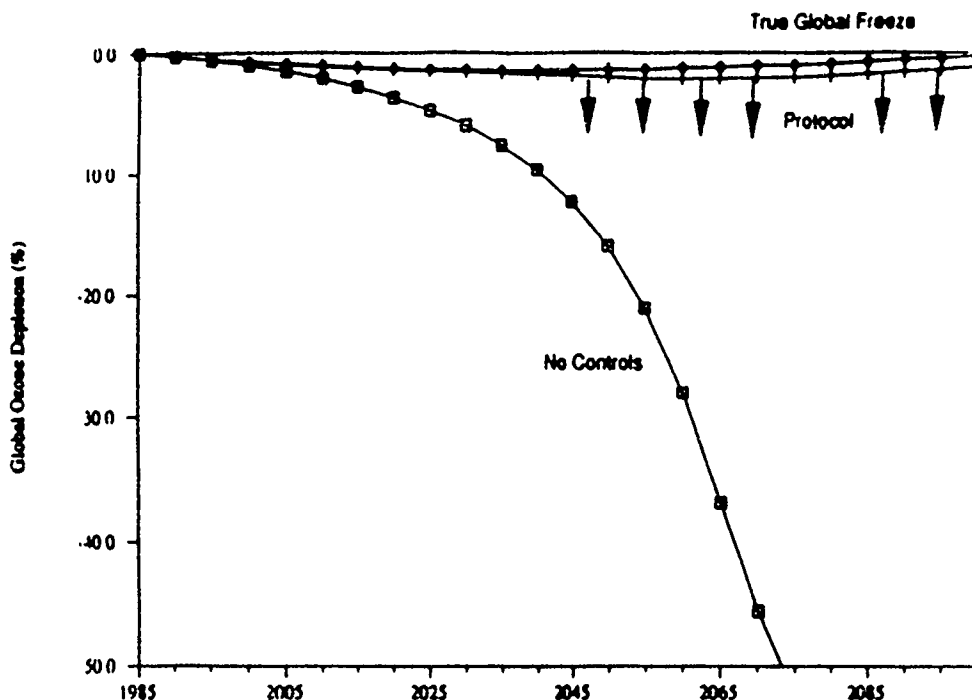
Assumptions:

No Controls: Compound use grows at an average annual rate of 2.8 percent from 1985 to 2050, with no growth thereafter.

Protocol: U.S. participation; 94 percent participation in other developed nations; 65 percent participation in developing nations. Use of compounds not covered by the Protocol grows at the rates in the No Controls scenario. Growth rates among non-participants are reduced to 37.5 percent (developed nations) and 50 percent (developing nations) of their baseline values.

True Global Freeze: The use of all chlorine-containing compounds is frozen at 1986 levels starting in 1990, and 100 percent participation is achieved worldwide.

Other Trace Gases: CH4 grows at 0.017 ppm/year; N2O grows at 0.2 percent/year; CO2 grows at the 50th percentile rate reported by the NAS (about 0.6 percent/year).

Arrows indicate that ozone depletion estimates may be underestimated.

FIGURE 2. OZONE CHANGES WITH VARYING CONTROLS.

MONTREAL PROTOCOL

The Montreal Protocol on Substances That Deplete the Ozone Layer was signed by 24 nations on 6 September 1987. Forty-five countries have signed to date. Countries representing over two-thirds of global production have ratified the Protocol, which enters into force 1 January 1989. The Protocol defines eight specific materials (which are separated into two groups) and a control schedule for these materials. A freeze in CFC (group I) consumption levels is called for. In May of 1989, a call for scientific review of atmospheric data will be made. If significant evidence is found indicating a worsening of the ozone problem, the timetable, scope, and stringency of the Protocol may be tightened as early as May 1990. The current timetable is listed in Table 3.

The Basket Concept

The Protocol has called for a reduction in consumption levels of CFCs and halons. Using the ozone depletion potential, a producer may decide which materials within a group to freeze or reduce in production. The basket concept allows for substitution within a group as long as the total overall consumption is reduced. For example, a producer could choose to maintain the current production level of CFC-113 if a corresponding decrease in production of another CFC material is made.

AD HOC SOLVENTS WORKING GROUP

In March 1988, Dr. Stephen Andersen, Chief of the Technology and Economics Branch, Global Change Division, EPA, and a group of industry and military representatives convened. Table 4 shows the various groups represented as part of the Ad Hoc Solvents Working Group. The purpose of this initial meeting was to determine a way to evaluate alternative cleaning materials and implement them into manufacturing facilities as quickly as possible. A comprehensive test program was needed to evaluate the performance of new cleaning materials and processes. It is also important to examine the environmental, health, and safety issues of the alternative materials.

Current military specifications limit the type of cleaning materials allowed. One of the major stumbling blocks to the acceptance of alternative cleaning materials is the amount of time required to alter a specification. The military specifications are considered as industry standards. It was the consensus of the group to plan a research project of which the military would approve and in which it would participate. Early in the planning stages, a briefing was held at the Pentagon to inform military representatives as to what the Ad Hoc Solvents Working Group had planned. The military concurred with the plan and gave the go ahead, promising to be responsive when the time came to modify the appropriate specifications. In a letter dated 18 May 1988, Mr. Peter Yurcisin, Office of the Assistant Secretary of Defense, Production and Logistics, Director Standardization and Data Management, stated that his office would "serve as a clearing house for DOD and military service review and will be the contact point for formal acceptance of the final plan." (Reference 5) At this meeting, Dr. Donald Fox, Office of the Secretary of Defense, said if the use of alternatives and substitutes for CFC-113 provides equal or better performance characteristics and at the same time protects the environment then it is an all-win situation

TABLE 3. MONTREAL PROTOCOL PROVISION SUMMARY AND TIMETABLE.

Group I - Fully Halogenated (CFCs)	Group II - Halons
CFC - 11 ($CFCl_3$)	Halon - 1211 (CF_2BrCl)
CFC - 12 (CF_2Cl_2)	Halon - 1301 (CF_3Br)
CFC - 113 ($C_2F_3Cl_3$)	Halon - 2402 ($C_2F_4Br_2$)
CFC - 114 ($C_2Cl_2F_4$)	
CFC - 115 (C_2ClF_5)	

Entry into Force - 1 January 1989, or when 11 countries (or 2/3 of 1986 global consumption) ratify Protocol.

Group I - Fully Halogenated CFCs

1 July 1989 - Freeze at 1986 production levels

1 July 1993 - 20% Reduction of 1986 production levels

1 July 1998 - 50% Reduction of 1986 production levels

Group II - Halons

1 February 1992 - Freeze at 1986 production levels

Trade controls

All CFC and halon bulk imports will be banned on 1 January 1990.

All CFC and halon exports will be banned 1 January 1993.

All listed products containing CFCs and halons will be banned within 3 years of entry into force (1 January 1992).

A ban is being considered for products made with, but not containing, CFCs and halons within 5 years of entry into force (1 January 1994).

.·.· ·. AD HOC SOLVENTS WORKING GROUP PARTICIPANTS.

<u>Solvent/Alternative Chemical Producers</u>
Allied-Signal
Du Pont
ICI Chemicals
Petroferm
DuBois

<u>Flux/Equipment Manufacturers</u>
Alpha Metals
Electrovert
Kester Solder
London Chemical
Stoelting
Unique Industries
Forward Technologies
Exxon Chemical

<u>Defense Contractors</u>
General Dynamics
Honeywell
Hughes Aircraft
IBM ·
Texas Instruments
Litton
Boeing

<u>Manufacturers</u>
AT&T
Digital Equipment
Ford
Northern Telecom
Magnavox

<u>Government Agencies/Other</u>
EPA
U.S. Army
U.S. Air Force
DOD
Navy - Electronics Manufacturing Productivity Facility (EMPF)
Navy - Naval Avionics Center (NAC)
Underwriters Laboratories
SANDIA National Laboratories
Robisan

<u>Industry Association</u>
Institute for Interconnecting and Packaging Electronic Circuits

which can expect the complete support of DOD. Deputy Assistant Secretary of Defense (Environment) Parker pledged prompt acceptance of new cleaning processes at a United Nations Environment Program meeting at the Hague.

A Test Verification and Monitoring Team (TVMT) was established to attend some portion of the testing and validate test results. Table 5 lists the members of the TVMT. This TVMT becomes especially important in Phase II when multiple test sites are allowed. A minimum of five members (one from each major group) is required for observation of testing.

The Ad Hoc Solvents Working Group developed a three-phase program. Each phase is outlined below.

Phase I: Benchmark Testing

a. The screening test is a dry run of testing to determine problems with the fluxing and assembly procedure.

b. The cleaning of standard printed board assemblies using an existing nitromethane stabilized CFC-113/methanol azeotrope to establish a benchmark reference value.

c. Announcement of benchmark test results.

Phase II: Limited Alternative Cleaning Media Evaluation

a. Selection of a limited number of test facilities.

b. Selection of alternative cleaning media.

c. Cleaning of standard printed board assemblies using the selected alternative cleaning media for comparison with benchmark.

Phase III: IPC Round Robin Program

a. Review of benchmark results and limited alternative cleaning evaluation.

b. Modification of the test plan if required.

c. Determination of the mixture of fabrication, assembly process, cleaning materials, and cleaning processes for evaluation to reduce variables for test.

d. Develop industry standard cleaning/cleanliness evaluation protocol.

e. Run round robin test.

f. Develop cleanliness acceptance criteria for assemblies for various (Classes 1, 2, and 3) usage environments.

TABLE 5. TEST VERIFICATION AND MONITORING TEAM.

Chairman - Leslie Guth, AT&T

Industry Liason - David Bergman, IPC

EPA Liason - Stephen Andersen

Service Representation

    Army - Carl Buchanan
    Air Force - Luke Lorang
    Navy - EMPF - Kathi Johnson
    Navy - NAC - Robin Sellers
    NASA - Felix Crommie

User Representation

Commercial

    AT&T - Leslie Guth
    Ford - Peter Sinkunas
    Northern Telecom - Dennis McCulloch

Military

    Boeing - Ron Janott
    Magnavox - Phil Wittmer
    IBM - Fred Freiberger
    Texas Instruments - Joe Felty

Supplier Representation

Chemicals

    Allied - Kirk Bonner
    Alpha - Al Schneider
    Du Pont - Bill Kenyon
    ICI - David Hey
    London Chemical - Alan Wang
    Petroferm - Mike Hayes

Equipment

    BBI - Michael Ruckreigel
    Detrex - Don Gerard
    Electrovert - Don Elliot
    Unique Industries - Art Gillman

BENCHMARK APPROACH

To characterize the performance of new alternative cleaning materials and processes, it was necessary to establish the performance of an existing CFC-based cleaning material as a benchmark data set. This benchmark data set would be used for comparison to the alternative cleaning materials and processes. Each new cleaning process must have results which equal or improve the benchmark test results.

An industry standard test assembly was designed to generate data evaluating both through-hole and surface mount technologies. A drawing of the test board is shown in Figure 3. The board is configured on 0.060-inch thick FR-4 laminate, with overall dimensions of 4 inches by 4 inches. The board is divided into four quadrants. Via holes are included on two of the quadrants to allow the maximum amount of flux to flow up underneath the components during wave soldering thus mimicking current through-hole technology. The via holes are linked together in a daisy chain pattern to obtain Surface Insulation Resistance (SIR) data. The other two quadrants of the board, representing surface mount technology cleaning challenges, have pairs of conductor lines of equal length inside and outside of the component land areas to facilitate post cleanliness evaluation by SIR. Comb patterns have also been incorporated underneath the components for each quadrant. Only one pattern of each pair will be populated with a component.

Two 68-pin leadless ceramic chip carriers (without internal circuitry), 0.050-inch pitch, will be placed on each test assembly. Guard traces have been added to the test board design to minimize leakage currents during electrical measurements. A fixed standoff was incorporated into the board design. This standoff consists of a copper pad (0.060-inch diameter) and a solder mask dot (0.040-inch diameter). The total height of the copper pad and the solder mask is 0.005 inch. (Artwork for this test board--number IPC-A-36-- is available through IPC. Northern Telecom is also making the test boards and components commercially available for those that want to do some testing in-house.)

Ionic cleanliness, residual rosin, and SIR tests are required for Phase I of the program. The ionic cleanliness test will quantify the amount of residual ionic contamination on the test assembly after each assembly sequence. Quantifying the amount of rosin remaining on the test assembly after each assembly sequence will be done with the residual rosin test. The SIR test is very complex. A voltage is applied to two conductive traces that are closely spaced. The SIR value obtained relates to the current leakage between the conductive traces. Ten measurements are required for each test assembly. These ten measurements correspond to the different traces on each board.

Assembly materials (flux and solder paste) were selected to provide higher than normal quantities of contamination on the test assembly so a discrimination of marginal processes would be easier to determine. Rosin Activated (RA) flux and RA solder paste were used. Other assembly processes were selected, not necessarily as the best process, but as the easiest to control and reproduce. It is anticipated that this test process will be duplicated many times and therefore consistency of process was a primary concern. In Phase I, assembly sequences A through D (Figure 4) were repeated to ensure replication of the data.
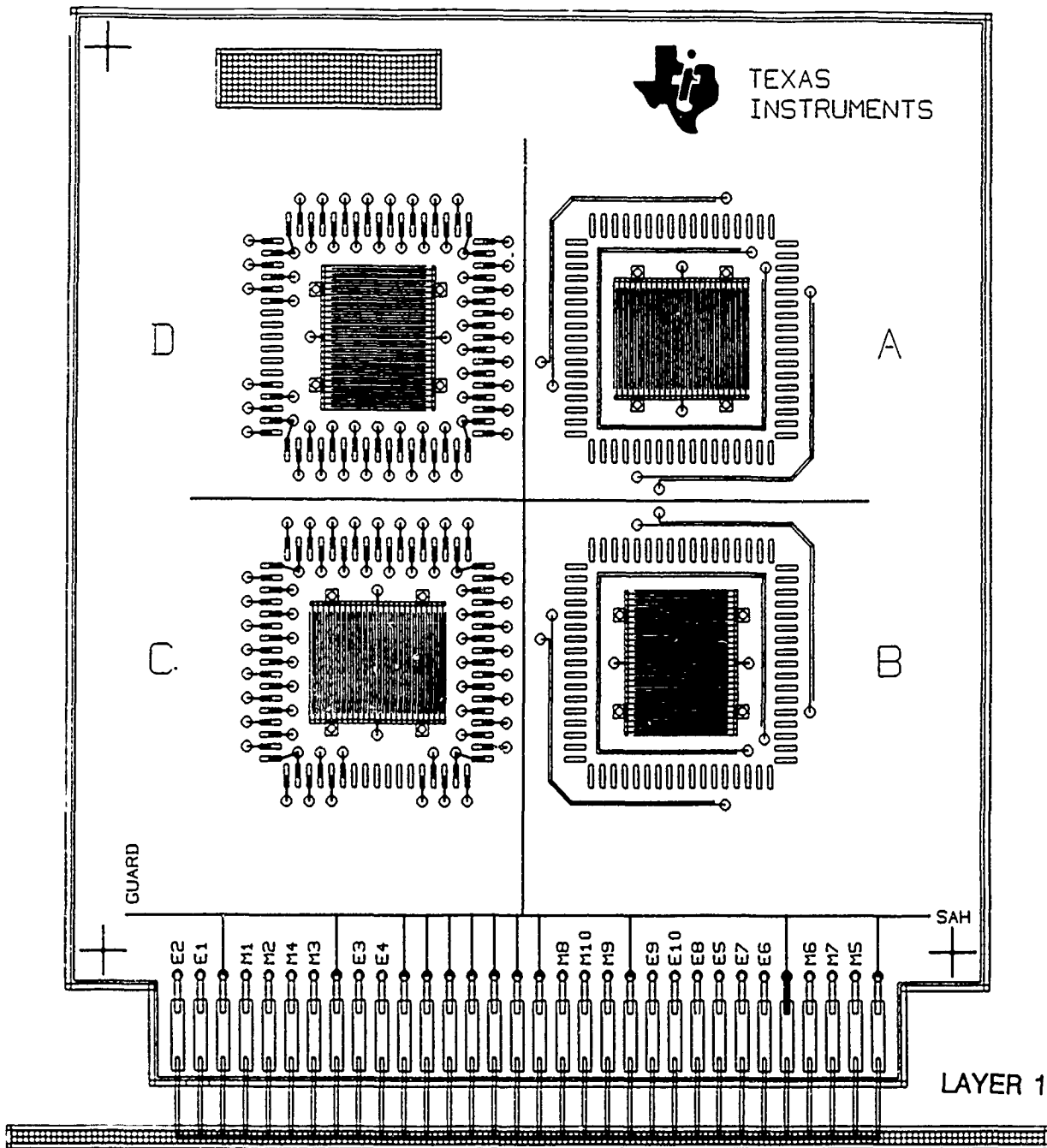
FIGURE 3.   CFC TEST BOARD DRAWING.
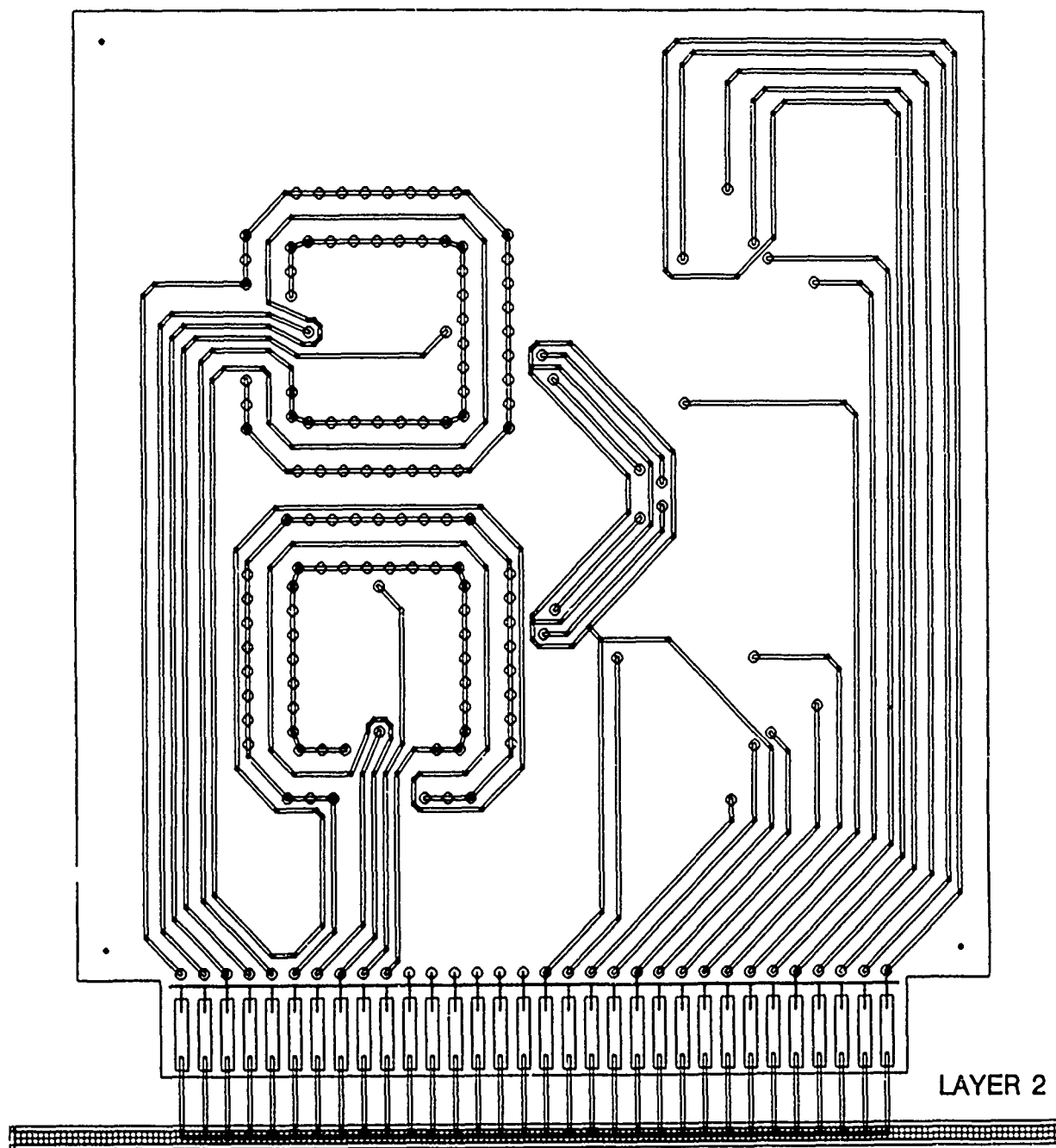
FIGURE 3.   CFC TEST BOARD DRAWING.
(Continued)
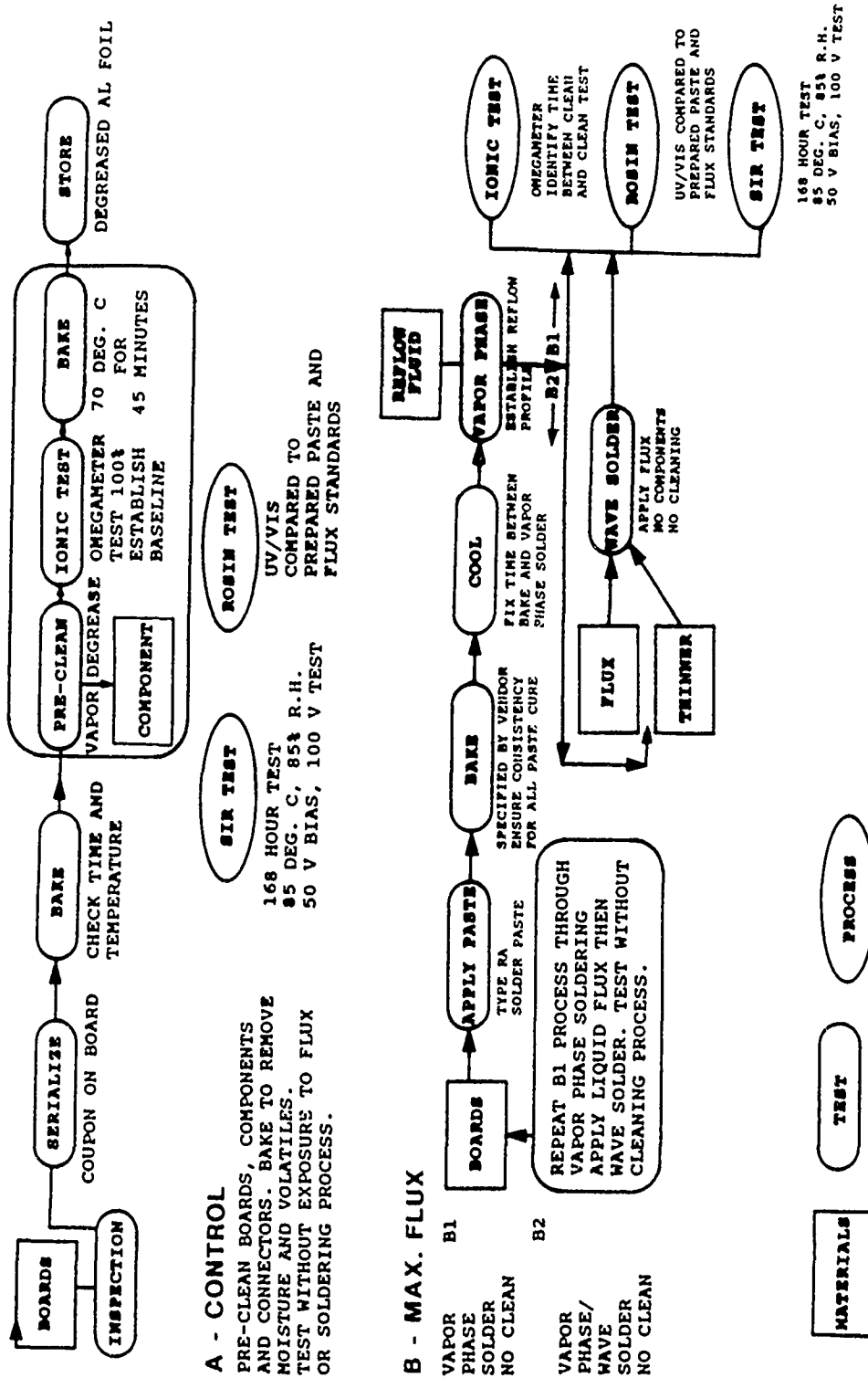
LAYER 2
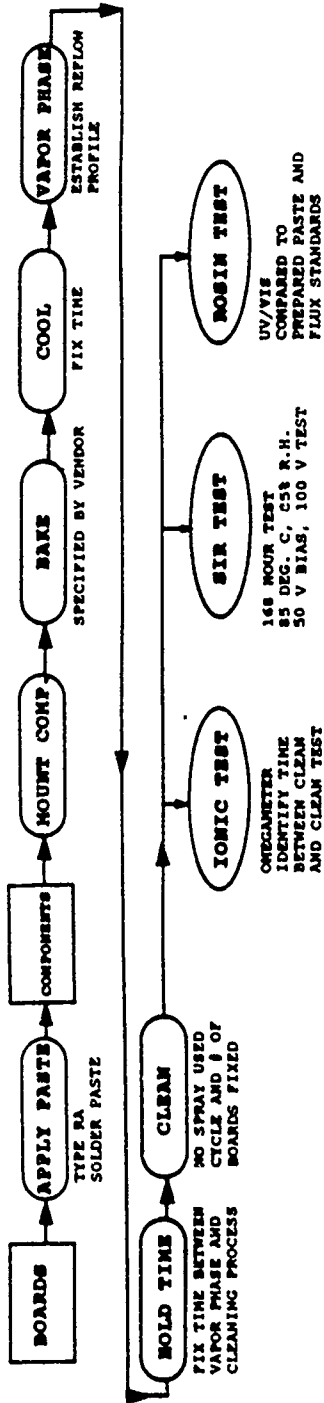
FIGURE 4. FLOW CHART OF TEST ASSEMBLY SEQUENCES.
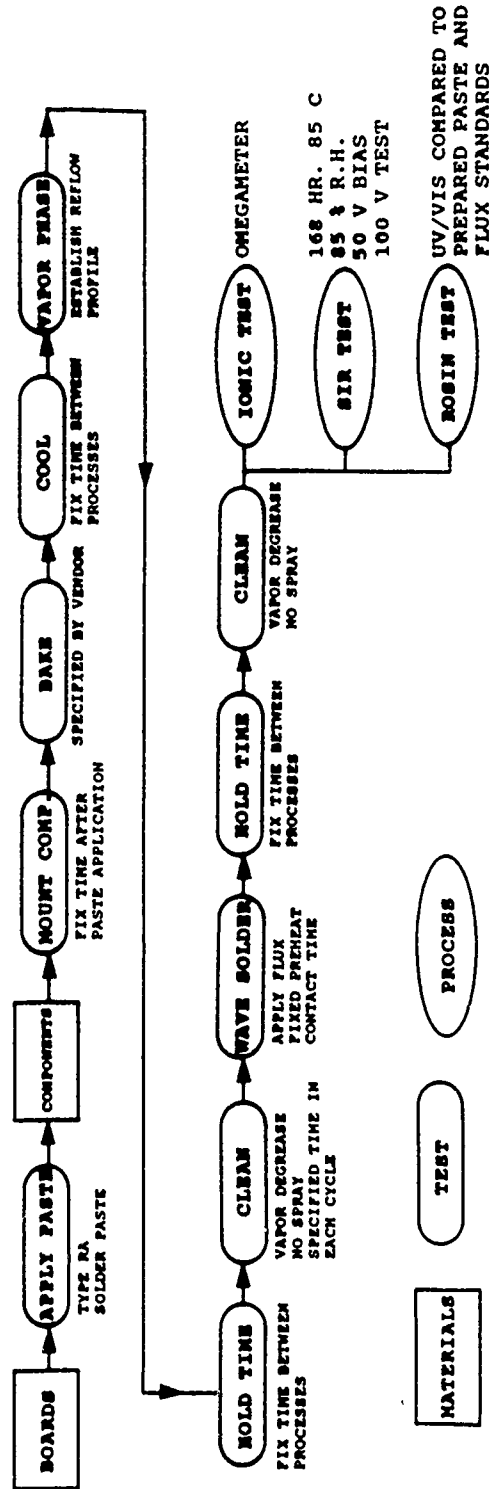
FIGURE 4. FLOW CHART OF TEST ASSEMBLY SEQUENCES.
(Continued)

PHASE I

The Electronics Manufacturing Productivity Facility (EMPF) was selected as the primary test site for the Phase I testing. The EMPF is a Navy facility that performs research in electronics manufacturing materials and process controls. Additionally, the Naval Avionic Center (NAC) was selected to repeat the benchmark testing using the same processes but different equipment. All of the materials required to perform this test were donated. The support from industry to contribute to, and participate in, the research effort to identify viable CFC alternatives was outstanding. A list of the materials, their providers, and/or support is listed in Table 6.

The specific requirements of the test program are included in the IPC publication *Cleaning and Cleanliness Testing Program - A Joint Industry/Military/EPA Program to Evaluate Alternatives to Chlorofluorocarbons (CFCs) For Printed Board Assembly Cleaning*, dated 30 November 1988.

In many cases, further definition of the process was required to ensure later duplication of the process. Each process was defined and controlled during the process development portion of the testing. The result of the process development was to minimize any fluctuation in processes or unexpected delays during actual benchmark testing. The benchmark testing is divided into five assembly sequences. Figure 4 illustrates a flowchart of the benchmark tests. Test A is included as a control. For the control test, the unpopulated test board was not exposed to any paste, flux, or soldering operation. Data was obtained for ionic contamination, residual rosin, and SIR to characterize the initial condition of the test assemblies after bake and precleaning processes only. Test B, or the maximum flux test, is composed of two parts labeled B-1 and B-2. This test will provide data for the worst-case scenario--no cleaning. Test assemblies are prepared using solder paste and vapor phase reflow alone for B-1, and vapor phase reflow followed by wave soldering for B-2. Tests A and B will provide the two extremes, best and worst cases for the benchmark test process. It is anticipated that the results of tests C and D will fall between these two extremes.

The assembly sequence for test C used populated test assemblies, vapor phase reflow, and cleaning with a batch vapor degreaser. Test data is again collected for ionic contamination, residual rosin, and SIR. Test assemblies for test D are prepared using both vapor phase reflow and wave soldering processes. Again, cleaning with a batch vapor degreaser is performed prior to testing.

During the development of the test plan, there was much discussion concerning the inclusion of a visual examination as part of the benchmark testing. It was decided to perform some visual examination of the test assemblies, but not as part of the test plan. A sample of test assemblies from the various assembly sequences will be inspected, disassembled, and photographed.

Another test that was not formally included in the test plan is High Performance Liquid Chromatography (HPLC). This test method is being developed to further characterize residues remaining on the test assembly which cannot be detected by the other test methods included here. The HPLC method may be formally incorporated into Phase II or III of the test program.

TABLE 6. DONATED MATERIALS AND SUPPORT.

Material/Support	Name	Company
Flux	Dennis Bernier	Kester Solder
Solvent	Bill Kenyon	Du Pont
Solder Paste	Norb Socolowski	Alpha Metals
Omegameter SMD600	Dick Carpenter Jerry Shultz	Alpha Metals
SIROMETER	Joe Rothenbach	Alpha Metals
Thermotron Humidity Chamber	Greg Miller Ed Nemic	Alpha Metals
Reflow Fluid		3M
Stencil	Ron Janott	Boeing Electronics
Stencil Frame	Jan Rigsby	Rigsby Screen and Stencil
Nest Plate	Mike Milam	Design Automation
CFC Test Board Layout and Artwork	Joe Felty	Texas Instruments
CFC Test Boards	Dennis McCulloch Art Fitzgerald	Northern Telecom
Components	Ray Prasad Jack McMahan	Intel
Wire	Jim Amesworth	Gore
Connectors	Wendy Herb Charles Brooks	AMP, Inc.
Engineering Labor	Ernie Lowe Barry Marcellus	Northern Telecom
Batch Vapor Phase Reflow System	Harold Hyman	Dynapert

TABLE 6. DONATED MATERIALS AND SUPPORT. (Continued)

Material/Support	Name	Company
Batch Vapor Degreasing System Maintenance	Carl Koenig	Allied-Baron-Blakeslee
Solder Paste Screen	Bob Mattson Art Gillman	Unique Cleaner Industries
Process Development Testing Support	Jim Maguire Doug Pauls Bill Groft Emery Gorondy	Boeing NAC Du Pont Du Pont
Data Analysis Software	Phil Wittmer	Magnavox
Process Checklists	Philipp wh Schuessler	IBM

In order to standardize the format for the results, a data analysis plan was prepared. This plan included a format for how the data should be collected, what analysis of the data was required, and how the results should be formatted and plotted. A sample size of five test assemblies was used for each assembly sequence and test. For each A through D assembly sequence run, a minimum of 99 test assemblies were required. Table 7 provides a breakdown of test assembly quantities needed for each test.

PHASE II

The two-fold purpose of Phase II is to (1) evaluate and find CFC alternatives that make the greatest positive impact on stratospheric ozone protection, and (2) maintain cleaning performance and environmental standards. Benchmark testing specified in Phase I will be duplicated for CFC alternatives, with the exception of the cleaning process. The alternative cleaning material and processes will be substituted in place of batch vapor degreasing using CFC-113 material.

Representatives from the Defense Logistics Agency's Hazardous Material Minimization (HAZMAT) Program participated in the development of Phase II requirements. The HAZMAT program is one that encourages the up-front selection of materials for minimization of hazardous materials in military programs. At the September 1988 meeting, George Brunner, Defense Electronic Supply Center, HAZMAT Program Manager, discussed the need for environmental review of the CFC substitutes prior to acceptance by the military. This view was shared by all of the DOD representatives present. The recommendation from this program was that any alternative material should be assessed for environmental, health, and safety concerns. If an environmentally responsible CFC alternative is not found, we will be trading one environmental problem for another.

In order to evaluate materials expediently, multiple test sites will be used for Phase II testing. The four categories of test sites are listed below.

a. Material vendors
b. Independent military labs
c. Electronic assemblers
d. Independent test labs

All of these test sites must meet the test site evaluation criteria given in the following list.

a. Organization of supervisory and responsible test personnel.

b. Personnel records, including resumes and job descriptions, of supervisory and other personnel directly involved with the testing.

c. Training and retraining or competency assurance procedures.

d. Test Equipment and Facilities. There shall be adequate space, environmental controls, test equipment, and safety systems provided.

TABLE 7. TEST ASSEMBLY REQUIREMENTS.

Assume 250 boards and 200 components available for Phase I Testing

Process Development			Boards 52	Components 16
Process	Test	Qty. for test	Total	Components
A	SIR	5 each		0
	Rosin	5 each		0
	HPLC	3 each		0
	EXTRAS*	5		
			18	
B	Ionics	2 each	4	0
	SIR	5 each	10	0
	Rosin	5 each	10	0
	HPLC	3 each	6	0
	EXTRAS*	5		
			35	
C	Ionics	5 each		10
	SIR	5 each		10
	Rosin	5 each		10
	HPLC	3 each		6
	EXTRAS*	5		10
			23	46
D	Ionics	5 each		10
	SIR	5 each		10
	Rosin	5 each	10	10
	HPLC	3 each	6	6
	EXTRAS*	5		
			23	46
TOTAL for 1 test set			99	92
Repeatability			99	92
			198	184

* = May be able to reduce the number of extra boards needed.
   This will depend upon the success of production process.

e.   Test equipment maintenance and calibration procedures.

f.   Preparation, handling, control, and identification of printed board assemblies.

g.   Actual testing of printed board assemblies.

h.   Available reference standards and/or materials. *Cleaning and Cleanliness Testing Program - A Joint Industry/Military/EPA Program to Evaluate Alternatives to Chlorofluorocarbons (CFCs) for Printed Board Assembly Cleaning* dated 30 November 1988.

i.   Test reports.

j.   Test facility record keeping.

Qualification of a test facility to evaluate the cleaning of printed board assemblies shall be initially established and periodically reaffirmed thereafter by on site review. The TVMT may observe some or all of the testing and must approve the test report prior to publication. (Refer to Table 6 for members). It was generally agreed that all results of any material evaluated in Phase II would be published, regardless of the testing outcome. This policy will ensure that material vendors will perform preliminary tests.

There was some concern regarding material prioritization for review in Phase II. In response to this concern, a multitiered approach to material evaluation was developed. Materials that meet the following criteria would be considered in the first tier.

a.   Commercially available material.

b.   Material compatible with commercially available equipment.

c.   The Ozone Depletion Potential (ODP) must be at least 20% less than the nitromethane stabilized CFC-113/5% methanol azeotrope (i.e., O.D.P. less than 0.60).

d.   One material per company submitted for first tier testing.

A material vendor must also provide specific information to participate in Phase II testing. A detailed flow of the cleaning process including times, temperatures, dwells, and so forth is required. Additionally, information concerning toxicology studies, recommended waste minimization and handling procedures, and Material Safety Data Sheets (MSDS) must also be submitted. The deadline for submitting data for the first tier is 31 March 1989. Those materials that will be commercially available within one year and may require new equipment are included in the second tier. Finally, the third tier will include those material vendors that have already submitted materials in the first or second tier.

The test facility performing the testing is responsible for preparing a report of the test results. This report will be submitted to the TVMT for approval. Once this report is approved it will be sent to a DOD committee for review. This DOD committee has not yet been formed but will be comprised of representatives from all of the military services. The

DOD committee will review the results of the report and consider additional environmental, health and safety information concerning the alternative material. The DOD committee will then make a recommendation to the Office of Standardization and Data Management for specification revision. One of the first specifications that will be revised is the MIL-STD-2000 series. A recommendation will be made to the Soldering Technology Standardization Working Group. Publication of test results will be coordinated through IPC. (As of this writing, test results were not complete and therefore could not be published.)

PHASE III

Phase III will address many of the controversial cleaning and reliability questions that have existed for many years. These questions are being revisited because of the phase-out of CFC solvents. Some of the questions that Phase III will address are listed below.

a. What quantitative level of cleanliness is required for each type of technology?

b. If the solvents required to remove rosin based fluxes are no longer available, should additional flux chemistries, including water soluble and low solid fluxes be reevaluated?

c. Is it necessary to clean for all applications/end-use environments?

IPC will coordinate a round robin test to address these issues. The schedule for this testing has not yet been developed. IPC is looking for participants for Phase III.

CONCLUSION

The program has moved forward at an amazing pace. Phase I began in March 1987 and was completed in less than one year. It almost seems an understatement to say that it has been exciting to see so many people with such diverse backgrounds join together to participate in the program development and execution.

The benchmark testing is only the first step in addressing the cleanliness performance required from a CFC alternative cleaning material or process. The entire test program is important in that it is addressing a global problem and breaking new ground in establishing a means by which military specifications can be responsive to changes in technology.

As cleaning materials are tested using this approach, new technologies will evolve which provide more choices for optimizing the cleaning process. The result of this program will be a framework of testing which clearly states cleaning material requirements. In addition, the results will define how new materials should be tested and lay out the approval cycle for inclusion into military specifications.

REFERENCES

1.   *Executive Summary of the Ozone Trends Panel.*   Unpublished draft report. Information used by permission. 1988.

2.   United States Environmental Protection Agency, Office of Public Affairs. *CFCs and Stratospheric Ozone.* Washington, D.C., December 1987.

3.   United States Environmental Protection Agency, Office of Air and Radiation. *Future Concentrations of Stratospheric Chlorine and Bromine.*   EPA 400/1-88/005. August 1988.

4.   Federal Register Aug 12, 1988, Part IV, Environmental Protection Agency 40 CFR, Part 82, Protection of Stratospheric Ozone; Advanced Notice of Proposed Rulemaking.

5.   Peter Yurcisin. Letter to Dr. Steven O. Andersen. May 18, 1988. From the Office of the Assistant Secretary of Defense, Production and Logistics, Director Standardization and Data Management. Washington, D. C.

BIBLIOGRAPHY

Alliance for Responsible CFC Policy. *Press Advisory: Montreal Protocol on Substances that Deplete the Ozone Layer.* September 16, 1987.

Andersen, Stephen. *Chlorofluorocarbons in the Electronics Industry: A Use and Substitute Analysis.* Unpublished draft report; contents used by permission. United States Environmental Protection Agency, Office of Air and Radiation. Washington, D.C. EPA Contract No. 68- 01-7002. July 22, 1987.

Cleaning and Cleanliness Testing Program - A Joint Industry/Military/EPA Program to Evaluate Alternatives to Chlorofluorocarbons (CFCs) For Printed Board Assembly Cleaning Nov. 30, 1988. IPC.

Edelson, Edward. "The Man Who Knew Too Much." *Popular Science* January (1989): 6065, 102.

Executive Summary of the Ozone Trends Panel. Unpublished draft report. Information used by permission. 1988.

Federal Register Aug 12, 1988, Part IV, Environmental Protection Agency 40 CFR, Part 82, Protection of Stratospheric Ozone; Advanced Notice of Proposed Rulemaking.

National Aeronautics and Space Administration, National Oceanic and Atmospheric Administration, National Science Foundation, and the Chemical Manufacturers Association. *Airborne Antarctic Ozone Experiment Fact Sheet: Initial Findings from Punta Arenas, Chile.* September 30, 1987.

United States Environmental Protection Agency, Office of Air and Radiation. *Future Concentrations of Stratospheric Chlorine and Bromine.* EPA 400/1-88/005. August 1988.

United States Environmental Protection Agency, Office of Public Affairs. *CFCs and Stratospheric Ozone.* Washington, D.C. December 1987.

Yurcisin, Peter. Letter to Dr. Steven O. Andersen. May 18, 1988. From the Office of the Assistant Secretary of Defense, Production and Logistics, Director Standardization and Data Management. Washington, D. C.

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RESIDUE ON PRINTED WIRING ASSEMBLIES:

AN OVERVIEW AND A CASE HISTORY

by

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ABSTRACT

Residues associated with soldering operations are common throughout the electronics manufacturing industry. Prevention is necessitated by MIL specs which require soldered assemblies to be free of all residues. Because of the large number of variables which contribute to residue formation, residues frequently appear under seemingly constant conditions, and detailed understanding of the materials and processes involved is needed for corrective action implementation.

This paper presents the history of an investigation of white residue on solder masked printed wiring assemblies. The residue was determined to be flux related by experimentation and spectroscopic chemical analysis. Process modification testing was performed to evaluate the roles of flux identity, preheater temperatures, and several cleaning process variables. Assemblies were subjected to humidity and temperature cycling, including periodic examination and electrical testing.

Additionally, information learned during this investigation about a number of residue causes and cures is summarized.

INTRODUCTION

Stubborn residues associated with soldering form frequently on printed wiring assemblies and have been reported on modules, cable assemblies and connectors as well. These residues resist ordinary cleaning methods. Residues are often white, although yellow, brown, green, tan, purple, black and colorless residues also occur. Various residues are described as hazy, spotted, translucent, streaky, gummy, crystalline, filmy, embedded, or isolated on the surface. On printed wiring assemblies, residues may occur on solder mask, pads or traces, solder joints, laminate or components. Several manufacturers of circuit assembly and processing materials publish technical data sheets listing a variety of residue causes.

The purpose of this paper is to summarize the information obtained during an investigation of a white residue problem. An overview of general information about residues precedes the case history of identification and prevention of one type of residue.

SOLDERING RESIDUES OVERVIEW

This section summarizes information about the causes of soldering residues, the techniques used to analyze them, and the reliability issues associated with their presence.

RESIDUE CAUSES

Flux. Fluxes are perhaps the single most prevalent cause of residues. Although residues resulting from synthetic solvent soluble and organic acid fluxes have also been reported, rosin based flux is most commonly implicated.

Rosin is a natural product with over a hundred components, of which approximately 90% are the resin acids. The properties of rosin, including thermal stability, tendency to crystallize, ease of oxidation and solubility, are influenced by the ratio of components. This ratio in turn depends on geographical and climatic factors affecting the rosin source as well as processing by the flux manufacturer. The composition can also be altered by the flux user, particularly by heating which results in isomerization or oxidation of resin acids. Oxidized rosin is thought to be a common cause of difficult to remove residues.

Small quantities of activators are added to RMA and RA fluxes to increase their reactivity with metal oxides. Activators, including chloride and bromide, have also been detected in flux residues.

The traditional method used to remove flux residues is refluxing; assemblies are then heated and removed from the line prior to soldering, and then cleaned as usual. If the residue is primarily oxidized rosin or resin acid salts, the activated resin acids in hot flux are effective solvents. Other common removal methods include organic acids, mineral acids, alkalies, organic solvents and blends, and mechanical scrubbing.

Permanent Solder Masks. Residues and appearance changes that resemble residues are frequently associated with permanent solder mask materials. Errors in processing polymeric masks, particularly during formulation or during the curing cycle, may result in decreased chemical and physical resistance. Soft or porous mask material is more

difficult to clean and more susceptible to attack by the solutions encountered during soldering and cleaning. ANSI/IPC-SM-840, "Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards", provides test methods for evaluating the chemical and mechanical integrity of masks. The methylene chloride cure permanency test and pencil hardness abrasion resistance test cited in this specification may not always be completely reliable indicators of proper mask processing, but they are very simple to perform and can provide useful information.

Changes in the appearance of solder masks can resemble residues. Cracking, blistering, or flaking of the mask surface can cause a whitened appearance and may be due to excessive heat during mask cure or contamination under the mask. Cracking, surface defects or exposure to organic acid fluxes can cause exposure of the white mineral powder used as filler in some mask materials. It has been reported that solder mask which appeared normal upon receipt from the PWB manufacturer developed white discoloration following exposure to 160°F water; this was attributed to cracking and crazing of the mask surface which propagated during thermal stress. The initial surface defects were determined to be due to the board manufacturer's hot air solder leveling process.

Solder masks are dyed for inspection and cosmetic purposes. Bleaching of this dye by cleaning solutions can be mistaken for white residue.

Other Residue Causes. A variety of cleaning solution and process parameters have contributed to residue problems, even when the cleaning process is compatible with the other soldering operation materials. Degreasing solvents can leave residues if they are contaminated with excessive flux or if one component in a solvent blend is depleted due to evaporation or due to contamination by water. Halide ions resulting from degradation of halogenated solvents may form insoluble salts with solder or base metals. Insufficient replacement of aqueous saponifiers can cause a decrease in pH to an ineffective level or redeposition of saponified matter onto cleaned assemblies. Inadequate temperature control can reduce the solubility of surfactant in saponifier. The use of nondeionized tap water during aqueous cleaning has caused the formation of white residue. Undetected cleaning equipment failures, such as plugged nozzles or tank leaks, result in inadequate cleaning, and many soils become more difficult to remove as cleaning is delayed. Cleaning solvent may wick up under wire insulation, carrying flux residues with it; this is the common cause of "Green Crud", the copper salt of flux resin acids.

Materials and processes used in manufacture of the printed wiring board can cause residue problems during later assembly operations. Improperly cured laminate can react with flux, or can be sufficiently soft or porous to permit embedment of contaminants. Residual etchant chemicals, plating brighteners, and solder leveling oils may be incompatible with the post-solder cleaning process.

Components mounted on assemblies can be sources of residues or can be discolored giving the appearance of residue. Lubricants or waxes which leak out of components may not be removed by post-solder cleaning, and may be redistributed on the assembly during cleaning. Aluminum parts and holding fixtures react with alkaline saponifiers, forming a white product which may also be deposited on other parts of the assembly. Excessively high pH can oxidize solder as well, giving the appearance of a whitish residue.

Properly used, solder wave oil can eliminate some residue problems, but wave oil which is contaminated with flux can leave a stubborn residue. Other materials used in the soldering process which can leave residues are temporary solder masks, wash-away spacers, impure solder, lead cutting oils, and the protective coatings applied to component leads or boards to preserve solderability.

RESIDUE ANALYSIS METHODS

The solvent extract resistivity test for cleanliness required by MIL-P-28809 ordinarily will not detect residues, either because they are not soluble in the water/alcohol solvent mixture used, or because they are not sufficiently ionized to increase the conductivity of the test solution. A variety of analytical methods are used to characterize residues. These methods are not useful for routine QC purposes at this time because they are costly, time consuming, and yield primarily qualitative instead of quantitative data.

Microscopy and Scanning Electron Microscopy (SEM) permit visual evaluation of residues and the surface characteristics of solder masks or laminates. Used in conjunction with SEM, Energy Dispersive Xray (EDX) analysis provides identities and an indication of relative quantities of the elements present in a very small localized area, although EDX equipment commonly cannot detect elements whose atomic number is less than 9, or 5 in the case of some equipment.

Electron Spectroscopy for Chemical Analysis (ESCA), or Photoelectron Spectroscopy (PES), can detect the elemental composition (except hydrogen and helium) and give some molecular structural information about extremely thin surface layers of the specimen. Auger spectroscopy is another surface sensitive method occasionally used.

Fourier Transform Infrared Spectroscopy (FTIR) detects vibrational energies of the chemical bonds in the sample. This permits identification of functional groups within the molecular structure. For example, the presence of a carboxylic acid group, an ester linkage, or a carbon-carbon double bond can be confirmed. FTIR is the most useful method for characterization of unknown organic compounds.

High Performance Liquid Chromatography (HPLC) has been used to analyze residues. HPLC separates the various components of the residue and quantifies them. Dissolution of the residue in a solvent is necessary for sample preparation, and either known standard samples or subsequent further analyses are required for identification of the residue components.

RELIABILITY

Although accurate generalizations regarding the reliability impact of residues cannot be made due to the large number of residue types which occur, some consequences of the presence of residues, both immediate and latent, have been noted.

Often the presence of residues interferes with the adhesion of conformal coatings or other encapsulation materials. Contact resistance is increased by the presence of insulating residues, which can degrade performance or testability. Some residues such as flux activators are corrosive, particularly when exposed to humidity, high temperature, or voltage bias. Hygroscopic residues can accelerate corrosion by absorbing atmospheric moisture. The insulation resistance of insulating circuit materials such as solder mask or laminate may decrease when contaminated by residue.

It bears emphasizing that, again due to the tremendous variety of residue types, test results based on one type of residue cannot be extrapolated to other types.

CASE HISTORY

As is often the case, the residue problem discussed by this case history occurred inexplicably, unaccompanied by any known material or process changes. The other aspect which makes this a fairly typical case is that elimination of the initially discovered causes, flux and preheating, was not possible, and solution of the problem required further investigation.

This section describes the residue and the assemblies and processes involved in its occurrence, the effects of various process modifications and the selected corrective action, and the methods and results of the temperature/humidity cycling performed to assess the impact of the residue.

PROBLEM DESCRIPTION

The printed wiring assemblies (PWAs) which exhibited residue were solder mask over bare copper boards containing a moderate component population. The PWAs were subjected to a post-assembly bakeout, followed by wave fluxing, preheating, wave soldering, and conveyorized aqueous saponifier cleaning. Vapor degreasing was used for cleaning following solder rework. An additional degreasing, isopropyl alcohol wash, and aqueous saponifier cleaning cycle was performed prior to solvent extract resistivity cleanliness testing, bakeout and conformal coating.

The residue which resisted these standard cleaning methods was a white, spotty, somewhat grainy or powdery looking material. It occurred on the surface of the solder mask in randomly distributed splotches on both sides of the assembly. The residue could be mechanically scraped off and was not noticeable when wet.

The residue could be duplicated on test coupon boards containing no components when subjected to the entire soldering and cleaning process. Test coupons which were subjected to all aspects of the process except flux exposure did not develop residue. The identification of the residue was confirmed by ESCA; the major components of the residue were carbon, oxygen, tin, lead, and chlorine, typical of flux residues.

Although the processing and cure of the solder mask were investigated, the role of the mask material in this problem was not clear. Apparently some property of the mask allowed preferential adhesion of the residue. The mask on some boards exhibited what seemed to be inadequate chemical resistance when tested with methylene chloride, and it appeared that these boards tended to have larger amounts of residue. Most boards did not fail this test, and no other disorder in the properties or processing of the mask was found.

PROCESS MODIFICATION EXPERIMENTS

Testing was performed using solder masked coupons manufactured by an outside vendor simultaneously with production printed wiring boards (PWBs). No components were mounted on the coupons.

Flux Identity. Five flux types from three manufacturers were evaluated for residue formation. All were MIL-F-14256 type RMA fluxes. Brush application of flux was used for testing instead of wave application; all other aspects of the process sequence of bakeout, flux application, preheat, wave solder, and aqueous saponifier cleaning were identical to that used in production.

Flux identity was determined to be an important contributor to residue formation; three of the types tested produced sparse white residue, one produced a moderate amount, and one was a severe residue former. The two fluxes that had been in use during the occurrence of residue on production hardware were in the mild residue group.

Preheating. Optimal preheater settings had been established for each assembly type in production, targeting a topside temperature of around 200°F. When preheater settings typical of an average PWA were used, residue formed on the test coupons. Residue was prevented if use of the preheaters was entirely eliminated, and residue formation increased as preheater settings were increased. It should be noted that residue formation was visible after cleaning, but not visible following preheating or soldering prior to cleaning.

Precleaning of Boards. To rule out a contribution to the residue by a contaminant associated with the as received PWBs, test coupons were cleaned prior to undergoing the standard bakeout, solder, and cleaning cycle. Test coupons were cleaned by vapor degreasing, aqueous saponifier washing, isopropyl alcohol washing, or a sequence of all three methods. No precleaned coupon showed any reduction in residue formation compared with the control samples which were not precleaned.

Water Prewash. Soldered assemblies pass through four zones internal to the particular conveyorized aqueous cleaning system used. These zones are: clear water spray prewash, recirculating water/saponifier solution sprays, clear water spray rinsing, and drying by air knives and lamps. All water is deionized to greater than 20 megaohm-cm resistivity and is approximately 140°F.

It was determined that test coupons placed on the conveyor after the clear water prewash zone did not develop residue. Minor plumbing modification of the equipment provided a method to turn the water prewash sprays off or on, preventing or permitting residue formation respectively. Further experimentation demonstrated that residue formation could be prevented even with the water prewash turned on if the bulk of the flux was removed prior to water exposure, either by isopropyl alcohol washing or vapor degreasing and hot solvent spray.

The clear water prewash was eliminated for processing of production PWAs, which prevented formation of this particular white flux residue.

TEMPERATURE/HUMIDITY TESTING

Three groups of production PWAs were subjected to temperature and humidity testing to evaluate the effect of the presence of this residue. The groups were:

1. Five PWAs which had residue randomly distributed on both sides.
2. Five PWAs from which residue had been removed using brush scrubbing with water/saponifier solution.
3. Five PWAs without visible residue.

All PWAs were conformally coated and electrically tested prior to temperature/humidity exposure.

Temperature and humidity testing was performed in accordance with MIL-STD-810, Method 507.1, Procedure IV, Steps 1, 2 and 5 as required by the specification for the equipment being tested, except that ten 24-hour cycles were used. Each cycle varies between 30°C and 60°C at greater than 95% relative humidity. The assemblies were removed from the test chamber following one day, five days, and ten days; visual inspections were made and electrical tests were performed within two hours of removal from the chamber.

No visual evidence of corrosion was detected on any test PWA, nor was any increase in or reappearance of residue seen. On a few specimens with residue, the residue was more difficult to see after testing, and it remained less visible following a bakeout. No electrical anomalies or failures occurred on any of the PWAs tested.

CONCLUSION

One type of white post-soldering residue which resists ordinary cleaning methods is a flux residue, apparently due to interaction between heat-modified mildly activated rosin flux and deionized water. The occurrence of this residue did not accompany any known process change; it may have been due to a variation in the composition of rosin in the flux. Elimination of the clear water prewash step in the conveyorized aqueous cleaning system, so that soldered assemblies first encounter saponifier solution instead of plain water, effectively prevents the formation of this type of residue. Elimination of preheating of fluxed assemblies also prevents residue formation, but is not consistent with other aspects of efficient soldering. It was also observed that different RMA fluxes exhibited variable tendencies to form this residue.

BIBLIOGRAPHY

Dennis Bernier, Kester Solder, Des Plaines, IL, "The Nature of White
        Residue on Printed Circuit Assemblies".*

J. Gordon Davy, Westinghouse Electric Inc., Manufacturing Systems and
        Technology Center, Columbia, MD, "Tan Residue from Cleaning Rosin
        Flux from PWA's with Fluorocarbon Methanol Azeotrope".*

John Evans and Cynthia Parmer, Rockwell International, Collins Defense
        Communications, Cedar Rapids, IA, "Discoloration of Solder Mask on
        Hot Air Leveled PWBs: Mechanism and Effects", Rockwell working
        paper published by Government and Industry Data Exchange Program
        (GIDEP), June 1985.

Joe Felty, Texas Instruments, Dallas, TX, untitled paper providing
        three examples of white residue.*

Rudy Klima, Allied Signal Corp., Melrose Park, IL, "Analysis of White
        Residue by High Performance Liquid Chromatography".*

T.A. Krinke and D.K. Pai, Control Data Corp., Government Systems
        Manufacturing, Minneapolis, MN, "White Residue on Circuit Card
        Assemblies".*

Quynhgiao Le, Boeing Electronics, Seattle, WA, untitled paper providing
        a white residue case history.*

Alvin F. Schneider, Alpha Metals Inc., Newark, NJ, "White Residue
        Problems on Soldered Printed Circuit Boards".*

Warren Steinacker, Freon Products Laboratory, E.I. du Pont de Nemours &
        Co., Inc., Wilmington, DE, "DuPont's Field Experience in Prevent-
        ing White Residues".*

GIDEP Alert CK-A-87-01, "Wire, Hookup, Insulated, Stranded"

GIDEP Urgent Data Request UDR U9-U-82-04, "Wire and Cable;
        Compatibility of Materials"

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*Papers noted with an asterisk were presented at "An Organized Approach
 to Solving White Residue Problems", workshop co-sponsored by the
 Electronics Manufacturing Productivity Facility and the Institute for
 Interconnecting and Packaging Electronic Circuits (IPC), at IPC 31st
 Annual Meeting, April 22, 1988.

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DESIGNING AND PROCESSING PRINTED CIRCUIT LINES FOR CLEANABILITY

By

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ABSTRACT

A great deal has been published regarding the effectiveness of various cleaning agents. They have been compared to others in the same chemical class, such as solvent versus solvent, as well as to other classes such as solvent versus aqueous. Likewise, studies have been conducted to demonstrate the relative efficiency of numerous equipment designs. Frequently, however, process engineers may overlook the possibility. that combinations of cleaning agents and equipment that may work well for most PWB designs, may not provide acceptable cleanliness for others. Therefore, to provide for optimum cleanability, a study was undertaken to ascertain if the choice of material brands of types within a certain class, such as solder creams, have an effect on the product's cleaning properties. The results will be combined with previous studies of the relative effectiveness of cleaning agents and equipment designs, to provide for comprehensive optimization of cleanability.

BACKGROUND

The design of a cleaning process and the choice of fabrication chemicals for any new electronic assembly manufacturing endeavor, or for any such production facility that is being moved or given a new lay-out, is most often a carry-over of the processes and chemicals used on previous occasions. At the same time, evolving hardware designs that combine through-hole and surface-mounted technology with other features that impede cleaning, such as large, flat processor chips, massive heat sinks, RF guards, and various types of connectors, has resulted in many printed circuit designs that are very difficult to clean properly.

Most often, cleaning is designated a "unit operation" unto itself by process engineers, and is treated as though the cleaning process is independent of other manufacturing variables. By applying this philosophy, the cleaning process itself can be optimized, but the ultimate cleanliness of the product may well not be optimized, and maximum cleanliness of the product is the goal we seek. The ultimate cleanliness of printed circuit assemblies is a function of a number of factors. The cleaning unit operation can at best be "tailored" to the other factors, and this form fitting often may result in compromises and non-optimum combinations.

Some of the factors that combine to determine the cleanability of a printed circuit assembly are:

1. The hardware design (eg. heatsinks, size and shape of components, presence of transformers, connectors, etc.

2. The technology of the components (thru-hole, SMT, mechanical, etc)

3. The choice of soldering technique (ie. hand, wave, solder paste)

3a. The choices within the soldering technique, such as vapor phase or IR fuzing, oil injected wave vs dry, solder-cut-solder, type of wave, combinations thereof.

4. Selection of process chemicals: flux, solvents, pastes, temporary resists, wave oil, heat sink compounds, wire tacking and component staking adhesives, etc.

5. Selection of process equipment

6. Timing of the processes in relation to each other.

Several experiments were conducted to evaluate various methods and process chemicals for maximizing cleanability.

WAVE SOLDER FLUX EVALUATION

The first material examined was the choice of wave solder flux. The opportunity was also taken to also evaluate each flux for it's minimization of solder defects on actual product. Five fluxes with 35% solids and their respective thinners were acquired for the trial runs. A sixth was ordered and deferred until a month later for logistic reasons. The experiment is to repeated later with the same series of fluxes in their 15% solids form.

Each flux was installed on a wave solder line with specially trained statistical process control (SPC) inspectors, and was allowed to run for 5 to 10 days, depending on cleaning and defect rate problems encountered during the run. Seven defects considered to be soldering deficiencies, and which may be a function of the flux, were selected for counting. These were voids, insufficient solder, excess solder, bridges, pin (blow) holes, dewetting, and solder projections or icicles. Upon selecting a four-board sample, the time, flux density, solder temp, and bottom-side preheat temperature were recorded. During inspection (with gloved hands), the boards were examined for visible flux residue, and the MIL-P-28809 extract resistivity was conducted on the assemblies. All data was logged for the date and board part number. During the flux evaluations, no other variables were changed other than the board part numbers, which were all represented in each run, although in different numbers of each.

The results revealed that it was possible to combine good cleanability with minimal defects, even with the limited number of fluxes evaluated. It was also observed that one of the candidates exhibited a rather low defect rate, but allowed only marginal cleaning, while yet another exhibited both poor cleaning and defect rate. Obviously, if the only criterion for evaluation during this run was solderability, then the candidate with the good solderability but marginal cleaning may have been chosen. Also worth noting at this time is past experience that indicates some defluxing solvents vary considerable in their ability to remove all traces of flux residue depending on the particular flux being removed, and on the concentration of dissolved water in the solvent (800 to 1200 ppm causing white residue or incomplete removal almost invariably). To eliminate this variable in the flux evaluation experiment, a solvent was chosen that has been shown to be very tolerant to both flux changes and moisture absorption. The results are tabulated in figures one and two.

SELECTED RESULTS FOR PRO 1 BOARD

	Observations	Ave Defects In PPM	Av Ionic Residue IN uGm/Sq In.
1.	Bad odor	2,555	3.76
2.	Flux dried hard	690	6.20
3.	good foam & clean	896	5.1
4.	Difficult to clean	1,233	16.2
5.	Flux dried hard	739	12.04

SOLDER PASTE EVALUATION

To evaluate possible differences in the cleanability of the vehicles present in solder pastes, a similar test was conducted using solder pastes and leadless chip carriers. Previous tests have shown that the flux and vehicle in different solder pastes flow at a greatly varying rate. Whereas process chemists normally evaluate solder creams for the desirable processing properties such as stencilablilty, solder balling, tack, print definition, fluxing activity, etc. without regard to their possible detrimental affect of subsequent cleanability, this test was intended to determine the extent of flow-out of the vehicle, and the solubility of the after-solder residue of each of the candidate pastes. Seven pastes were chosen for preliminary screening. The preliminary flow-out determination consisted of stenciling circles of each past onto a clean ceramic substrate, which was then placed onto a hot plate that was running at 450 deg F. As the pastes warmed and softened, the spread rate and extent of spread was noted, and the diameter and color of the final flux ring after the solder had melted was measured and logged. (see photo #1). The largest extent of spread was 44% wider in diameter than the smallest, and the paste deemed best by other performance criteria had a diameter 36% larger than the paste deemed second best. (see photo #2)

To test the two latter solder pastes in actual applications, two different SMT configurations were fabricated from the top two candidates resulting from an evaluation conducted to source material for automatic pick and place machines. The first test consisted of a ceramic substrate with a 64-pin LCC mounted by stenciling solder paste on one side only, followed by IR reflowing. The LCC war then lifted, and the amount of flux migration was noted ar photographed. As before, the vehicle from the solder paste favored by the performance study flowed the entire length of one side and into the SIR pattern, whereas the second paste stayed relatively in place. Also noted was some scattering of solder balls resulting from the first paste, even on the bottom of the chip carrier.

A third test was conducted, again with the two top candidates as evaluated by other performance characteristics. This time six LCC's of varying sizes were mounted onto FR-4 laminate, two with SIR patterns under, and two without. After IR reflowing, the boards were photographed from the bottom side to show the soldering residue, which was visible through the laminate. Then a careful solvent extract resistivity test was conducted individually on each.

The boards were again passed through the IR oven with a profile designed to reach peak temperature just upon exiting the machine, and selected LCC's were removed. This time the area under the carriers were examined and photographed in ultraviolet light. Once again, this test indicated that the number one paste spread further and was more difficult to clean than the number two paste.

VAPOR PHASE PROCESS VERSUS INFRARED REFLOW PROCESS

It was decided to run a quick test similar to the preceding one to determine if LCC's soldered by vapor phase were more or less difficult to clean than if soldered by IR. To do this, four more FR-4 boards with six LCC's each were fabricated. Two had SIR patterns under the carrier, and the other two were blank underneath. One of the blank and one of the SIR boards was soldered in vapor phase and IR, using RA-type solder paste. As before, the boards were photographed from the bottom side to reveal the extent of flux migration, the solvent extract resistivity was determined, and again the boards were photographed. Finally some of the carriers were removed and the underside were examined and photographed under ultraviolet light. This series of tests was slightly less conclusive than the others. It is theorized that the vapor phase <u>does</u> cause the vehicle to flow under the carrier much more than does IR reflowing. However, the vapor phase fluid and CFC vapor blanket also flush off some of the flux, and leave the remaining residue less hard and more soluble in defluxing solvents. Conversely, the IR reflow does not cause the extent of spread as does the vapor phase, but it bakes the residue very hard and renders it less soluble in mild defluxing solvents. It was noted that both methods cause a "stain" or quenching of the board material's fluorescence, although the IR method has a much more pronounced stain. A separate series of tests is planned for the future to determine if this "stain" is detrimental to the board materials's insulation resistance or glass transition temperature.

SOLVENT VERSUS AQUEOUS CLEANING PROCESS

Tests In-house On SMD Configurations: Two tests were planned to access the viability of aqueous cleaning in lieu of solvent cleaning. In the first series, which was part of an IR&D program undertaken at Magnavox by M. Brownfield et.al., four commercially available saponifiers were evaluated by their ability to remove residual flux from four configurations of test boards, as well as wave oil from a glass plate.

The four boards were the standard IPC B-25 test board, a
Magnavox SMD test board, an SMD test configuration
consisting of six mounted LCC's as in previous tests above,
and an alumina ceramic substrate with a single 64-pad LCC
mounted. Also the minimum soak (spray) time for each
cleaner was noted, and the percent absorption in the board
material was determined. The cleaning was conducted in a
custom made device that incorporated the so-called
"impingment" principal, whereby the board lies just under
the surface of the liquid while a low to medium pressure
spray is directed on the top side. Each solution was used
at 10% concentration, and heated to 60 deg C. The flux
tests were meant to simulate bottom side SMD's, or top side
SMD's where via holes or other means allow wave solder flux
to penetrate under the carriers. Thus, the flux from the
solder paste used to mount the components was precleaned and
the test boards were ran in the Ionograph until the
instrument reached a stabile baseline. The results recorded
were residual ionic contamination (by ionograph), time to
clean the glass slide of residual wave oil (visual), minimum
time to clean the product to less than 20 micrograms per
square inch, and percent weight gain after the soaking
processes.

The results indicate that the saponification technique
cleaned all of the test configurations at least as well as
the CFC-113 defluxing blends in use at Magnavox, and did not
absorb significantly into the board, and could efficiently
remove mineral wave oil as well as rosin-based flux.

TEST RESULTS: AQUEOUS SAPONIFICATION EFFICIENCY FOR RA FLUX

* Time to clean glass plate of mineral wave oil (no visible
film) = 15 seconds (followed by a DI water rinse.)

* Retention of cleaning solution in laminate = +0.008% (ave)

TEST RESULTS; AQUEOUS SAPONIFICATION, CONT.

* Minimum time to clean RA flux from double sided, mixed technology board:

Seconds Immersion	Ionic Contamination, uGm/Sq.In.
5	19.5
10	15.3
20	4.8
30	5.0

* Minimum time to clean RA flux from under LCC on ceramic substrate:

Seconds Immersion	Ionic Contamination, uGm/Sq.In.
30	>20
40	18.5
50	10.5
60	1.6

* Ultimate cleanliness on various test vehicles:
  1. IPC B-25 boards, RA flux both sides, bake one hr. @ 120 deg C, then let stand overnight, then clean ====>1.6 uGm/Sq.In.

  2. Six LCC test board, pull vacuum while in flux, bake, stand overnight, clean ====> 11.7 uGm/Sq.In.

* Conclusions: The aqueous saponification technique cleaned the SMD configurations adequate to meet the cleanliness requirements of MIL-P-28809 and did not absorb significant amounts of the solution.

TESTS AT EQUIPMENT VENDOR ON MIXED TECHNOLOGY: Four Magnavox production boards and two test boards were taken to an equipment manufacturer's manufacturing technology center to evaluate the ability of an aqueous saponifier to remove RMA and RA flux, when compared to a stabilized azeotropic blend of FC-113/methanol. One of the production boards had bottom side SMD's (chip capacitors and resistors). Another had very large IC's and processors mounted with through-hole components, and a third from the same product line had traditional thru-hole components. The fourth was an older, very dense design with stand-up components and RF guards. The two test boards were the IPC B-25 board and the Six-LCC test board used in the previous tests above. All of the production boards were foam fluxed with RMA flux, and some had additional flux sprayed onto the top side.

They were then wave soldered at 4 fpm @ 500 deg F, and taken to one of two conveyorized cleaning machines, one with the aqueous saponifier and the other with the FC-113 solvent. The solvent cleaning machine was equipped with 200 psi spray as well as In all, four cleaning processes were evaluated, aqueous with and without DI water rinse, the solvent, and the aqueous line with a pre-dip in a terpene cleaner. The test boards were foam fluxed, or sprayed, or both, and then allowed to pass over the wave solder machines's preheaters, but were removed before the solder wave. They, too, were taken directly to one of the conveyorized cleaning machines. The cleanliness was evaluated by determining residual ionic material in an Omegameter SMD-600, an Ionograph 500, and by surface insulation resistance.

This series of tests generated many pages of data, and therefore only select averages of will be summarized herein. It was noted that the Omegameter SMD-600 yielded higher results than the Ionograph 500, and after some data reduction (which included disregarding two data 'flyers') it was decided to use an equivalency factor of 1.9 (ie., 20 uGm/Sq in the ionograph would equal about 38 uGm/Sq in the SMD-600). Because of their rather small size and the lack of agitation in the ionograph 500, the SMD configuration test boards were ran two times for 30-50 minutes on the advice of Alpha's Dr. Jack Brous, and the weight per unit area was summed for the two runs. The Surface Insulation Resistance was conducted by IPC Test Method 650, number 2.6.3, Moisture and Insulation Resistance, Rigid, Rigid/Flex, and Flex Printed Wiring Boards.

TEST RESULTS: SUMMARY OF CONVEYORIZED MACHINE AQUEOUS TESTS

Test Condition: No flux on top side.   Instrument: SMD-600

BOARD #	SOLVENT	AQUEOUS/DI	AQUEOUS/TAP
Board No.	uGm/Sq	uGm/Sq	uGm/Sq
53	22.5	27.6	32.7
A1	17.1	16.8	23.6
53/terpene	no data	19.8	no data

Test Condition: Top side flux: Instrument: SMD-600

53	no data	38.8	27.7
A1	18.5	20.6	30.3
53/terpene	no data	21.8	no data

TEST RESULTS: CONVEYORIZED MACHINE, CONT.

Test Condition: No flux top side. Instrument: Ionograph 500

BOARD #	SOLVENT	AQUEOUS/DI	AQUEOUS/TAP
53	6.7	12.9	24.7
A1	no data	2.1	no data

Test Condition: Top side flux: Instrument: Ionograph 500

53	no data	23.9	22.7
A1	no data	4.5	no data

IPC B-25 TEST BOARD SIR RESULTS

PROCESS	AVERAGE SIR
SOLVENT (FC-113/MeOH)	1.2E+11 OHMS
AQUEOUS/DI	2.4E+10 OHMS
AQUEOUS/TAP	1.5E+09 OHMS

SIX LCC SMD CONFIGURATION TEST BOARD SIR RESULTS

PROCESS	AVERAGE SIR	IONIC RESIDUE
SOLVENT, RMA PASTE	4.19E+12 OHMS	5.65 uGM/Sq In
SOLVENT, RA PASTE	5.75E+12 OHMS	20.2 uGm/Sq In
AQUEOUS, RMA PASTE	3.96E+12 OHMS	7.65 uGm/Sq In
AQUEOUS, RA PASTE	4.84E+12 OHMS	6.50 UgM/Sq In

The final portion of the data for maximizing the cleanability of PCB's during assembly was an evaluation of cleaning solvents currently in use at Magnavox, and available but not used. Obviously, it was quite impossible to evaluate all available solvents, so only those already in use, and candidates likely to provide improved cleaning were evaluated. None of the recently-introduced "Montreal Protocol" solvents were evaluated, simply because they were not available at the time the evaluation was taking place. Optimization of cleaning solvent properties was deemed necessary because of past experience indicating that the vast majority of occurrences of flux not being removed properly from PC assemblies were due to improper batch vapor defluxing after a hand soldering operation.

Again, this was a lengthy effort which involved ten solvents and eleven test protocols, and resulted in a sixty one page report. Thus, once again, only select portions will be summarized to illustrate the evaluation methods and reasoning. The following data summarizes: (1) the surface insulation resistance, residual rosin and ionic residues on IPC B-25 (Magnavox modified). RA flux was applied to the both sides of the boards, which were then baked at 110 deg C for one hour, and then allowed to stand overnight before cleaning; (2) A Six-LCC surface mount pattern without mounted carriers and with no SIR pattern under the component placements, but with residual flux from stenciled RMA solder paste; (3) 64-pad LCC's mounted on ceramic, with both solder paste flux residues and RA flux (applied after stenciling the paste but before mounting the carrier).

All samples were cleaned by immersing them into the vapor degreaser at 8 f.p.m. into the vapor over the solvent's boiling sump for 120 seconds, followed by a 4 second per side spray, and then clean sump immersion for 60 seconds, followed by another spray for 4 seconds per side. Next the samples were allowed to stand in the vapor for 90 seconds, and finally were raised to the freeboard area for 30 seconds to dry. The residual rosin was determined by a UV-VIS spectrophotometric method developed by Dow[1], the ionic residue was determined by an Ionograph 500, and the SIR was again determined by IPC TEST METHOD 6.5, number 2.6.3. The solvents are designated S1 thru S10, and are based on FC-113, FC-112 and 1,1,1-Trichloroethane, with other polar or halogenated ingredients added.

The results indicate that some FC-113 blends remove ionic residue very well, while leaving a significant amount of residual rosin, while others were more efficient at removing the rosin but not as good at removing ionic residue. There was at least one FC-113 candidate that was very efficient at removing both.

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1. Richey, W.F. and J.A. trombka, E.L. Tassett, T.D. Cabelka, A.H. Hazlitt; "New Analysis For Residual Rosin On Cleaned Electronic Circuit Boards", in Proceedings of the NEPCON WEST Conference, March 1985, Cahners Exposition Group

In general the 1,1,1 blends were more tolerant to processes that baked on the flux and to long dwell times between soldering and cleaning, although they varied widely in their ability to remove ionic soils. It should also be noted that while the FC-112 blend (#S-10) cleaned very well, it possessed enough isopropanol to exhibit a flash point below its boiling point.

RESULTS OF SOLVENT EVALUATION TESTS
FOR RA FLUX ON IPC B-25 MOD 1 BOARDS

Solvent No.	Ave. SIR	Residual Rosin,uGm/Sq	Ionic Residue,uGm/Sq
S1	5.85E+11	12.31	4.3
S2	8.82E+10	11.2	15.7
S3	6,83E+11	20.26	3.6
S4	2.99E+10	5.11	1.3
S5	2.88E+09	8.26	6.4
S6	1.84e+11	4.6	1.1
S7	3.83E+11	5.68	4.3
S8	3.47E+11	3.97	2.7
S9	1.49E+10	5.52	1.1
S10	1.35E+11	8.5	3.5

FOR RA FLUX ON CERAMIC WITH MOUNTED 64 PAD LCC's

Solvent No.	Ave. SIR	Residual Rosin,uGm/Sq	Ionic Residue,uGm/Sq
S1	4.40E+08	13.38	5.0
S2	8.80E+08	55.55	38.0
S3	1.96E+09	61.42	24.7
S4	2.82E+09	7.07	1.5
S5	2.15E+09	6.09	18.5
S6	1.87E+09	31.39	2.1
S7	1.20E+08	11.03	12.3
S8	7.71E+09	9.55	18.5
S9	2.40E+08	12.98	1.5
S10	5.50E+09	6.02	1.3

RESULTS OF SOLVENT EVALUATION TESTS, CONT.

FOR RA SOLDER PASTE ON SMD TEST PATTERN BOARDS

Solvent No.	Ave. SIR	Residual Rosin,uGm/Sq	Ionic Residue,uGm/Sq
S1	N/A	9.44	7.94
S2	N/A	12.73	9.6
S3	N/A	6.58	4.9
S4	N/A	5.71	3.3
S5	N/A	7.95	9.7
S6	N/A	5.76	3.4
S7	N/A	4.53	3.0
S8	N/A	5.67	1.8
S9	N/A	9.84	2.2
S10	N/A	3.87	2.6

CONCLUSION

This series of tests demonstrated that it was possible to select a wave solder flux, and a solder paste, and the method to reflow the solder paste, that would allow thorough cleaning in an aqueous medium. The tests also revealed the best choice of solvent for use in batch degreasers (defluxer) for post hand soldering operations. The tests also had the additional benefit of reducing the defect rate on wave soldered boards.

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REAL TIME LAMINOGRAPHY
Slicing Solder Inspection Down to Size

by

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ABSTRACT

The author presents the results of applying an automated real-time laminographic system to the inspection and process control verification of the solder quality of circuit board assemblies. Plated-through-hole, single-sided surface mount, mixed, and double-sided surface mount assemblies have been inspected using this new X-ray based technique that produces laminar X-ray slices (parallel to the plane of the board) through the soldered connection. The resulting set of laminographic images are much easier to analyze than a conventional X-ray image of the same area.

INTRODUCTION

Throughout the years, various technologies have been used to aid in the inspection of circuit card assemblies. These technologies varied from special microscopes and lighting for human inspectors, to automated X-ray inspection systems. The problem of monitoring, controlling, and maintaining board yield after the soldering process still confronts the industry. Additionally, as the density of connections on boards increases and as the device leads disappear under the packages, the industry standard of human visual inspection becomes even less reliable than it was with the older plated-through-hole technology. A new technology for solder quality inspection, called Scanned-Beam Laminography, is described in this paper.

THE NEED FOR A BETTER SOLUTION

The world's best circuit board production lines produce assemblies with a defect rate for soldering of around 50 parts-per-million (ppm). Reducing joint solder defect levels through process control feedback and inspection is extremely important. The board yield is a function of both the number of joints on the board and the defect rate at the joint level. For a given joint defect rate, the higher the joint count on an individual board, the lower the board yield (Reference 1). This is shown graphically in Figure 1. Board yields for boards containing 250 joints to 10,000 joints at joint defect levels of 10 to 500 ppm are calculated.
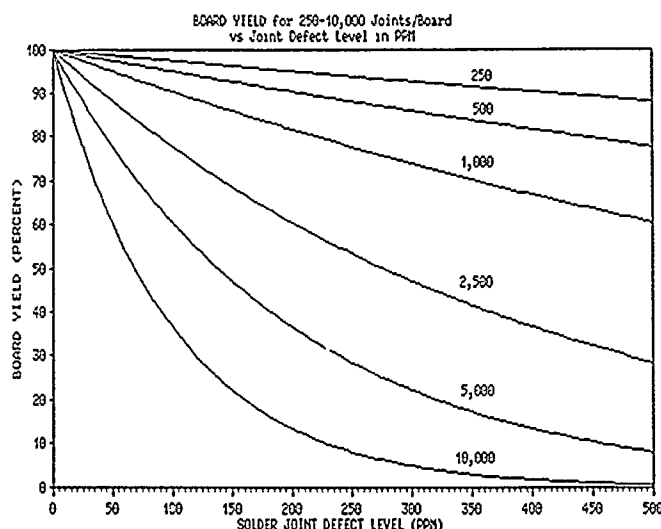
FIGURE 1. Board Yield Versus Defect Level.

The trend in manufacturing is toward more joints per board, therefore additional means must be employed to further reduce the process defect level. Even with further process improvements, statistical process control, and closed loop feed-back, many products will still require an inspection system to reduce the remaining defect levels to acceptable rates for product shipment.

FIGURE 2. Conventional Radiography.

The inspection system must also help in the rework loop by providing the proper classification of the defects it locates. Joints not requiring rework should not be "repaired." Reducing unnecessary repairs will ultimately be reflected in lower scrap rates, since repairs often cause board damage and necessitate scrapping.

The inspection system must also provide data in a timely manner to allow for close process monitoring and to flag any growing defect levels. Immediate corrective action limits the production of systematic defects and increases overall board yield.

Inspection systems in the past have met with some success for through-hole technology boards and for single-sided SMT boards (References 2-7). The most successful has been automated transmission X-ray (Reference 8), but transmission X-ray has problems with double-sided SMT due to the interference of the top-side components with the bottom side. Figure 2 shows a typical basic X-ray system. Note that the areas in the object labeled "A" and "B" overlap on the detector system, presenting an analysis problem. A new technology was needed.

SLICING THE PROBLEM DOWN TO SIZE

Just as Computed Tomography (CT) (Reference 9) revolutionized the medical diagnostic world by providing doctors with X-ray cross-section images of patients, Scanned-Beam Laminography (SBL) will provide a better way to examine soldered connections on circuit boards. The X-ray slice (CT) image allows doctors to diagnose medical problems without the "noise" associated with conventional transmission X-ray images. This "noise" is the intervening material between the desired slice to image and the material above or below it. In the early 1970's, Computed Tomography replaced an older cross-sectioning technique called laminography. CT gives the patient a lower X-ray dose and creates better images in a low contrast medium (the human body is basically about the same radiographic density), while laminography gives a better image when there are isolated areas of high contrast within a low-contrast medium (such as solder connections on circuit boards).
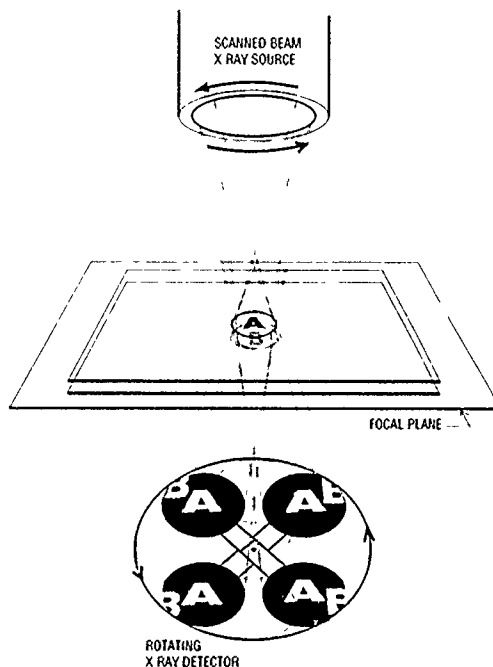
FIGURE 3. Basic Laminography.

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Laminography (References 10-13) was invented in 1922. When there is synchronized motion between the X-ray source and the detector, an X-ray slice image forms (Figure 3). Features (such as the letter "B" in the object) that are not in the plane of focus are projected to other parts of the detector and thus blurred as the source and detector move in a complete circle. Thus the "noise" from the letter "B" is eliminated when the system slices at the focal plane containing the letter "A."

Figure 4a shows a conventional transmission X-ray image of a double-sided SMT board with 50 mil pitch ceramic leadless chip carriers (LCC) mounted on both sides of the board. Figure 4b shows the laminographic slice taken at the top surface of the board and Figure 4c shows the laminographic slice taken at the bottom side of the board. These images clearly show solder balls around the pad area and voiding in the pads of some of the connections. Note that the internal structures of the package, the component on the opposite side, and the castillations, do not interfere with the slice image taken at the pad level.

FIGURE 4a. Conventional X-Ray Image.
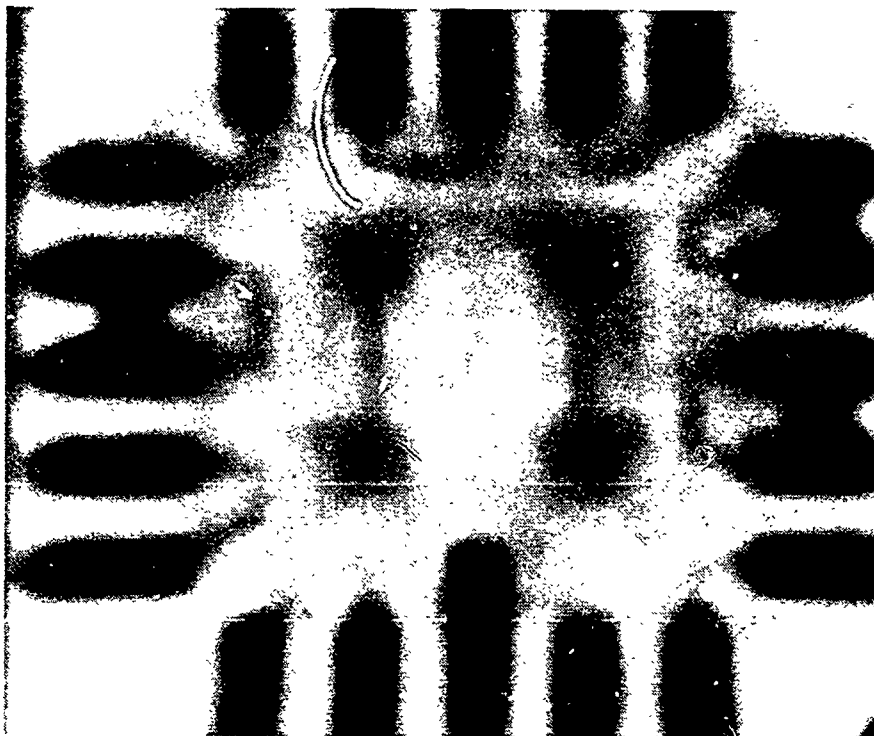
FIGURE 4b. Laminographic Image of Top of Board.

FIGURE 4c. Laminographic Image of Bottom of Board.

Mechanical scanned laminography, as used until it was basically abandoned in the early 1970's, is not suited for electronic solder inspection, since it takes a long time to generate a slice image (minutes), and the slice image is low resolution (on the order of 0.040 inch feature detection). Four Pi Systems invented a better way to generate laminographic images and has applied for patents. This new technology named Scanned-Beam Laminography (SBL) overcomes the mechanical scanning problems of the older laminographic systems. Scanned-Beam Laminography generates high resolution images (on the order of 0.001 inch) at high speed (100 millisecond per image). Basic Scanned-Beam Laminography is shown in Figure 5.
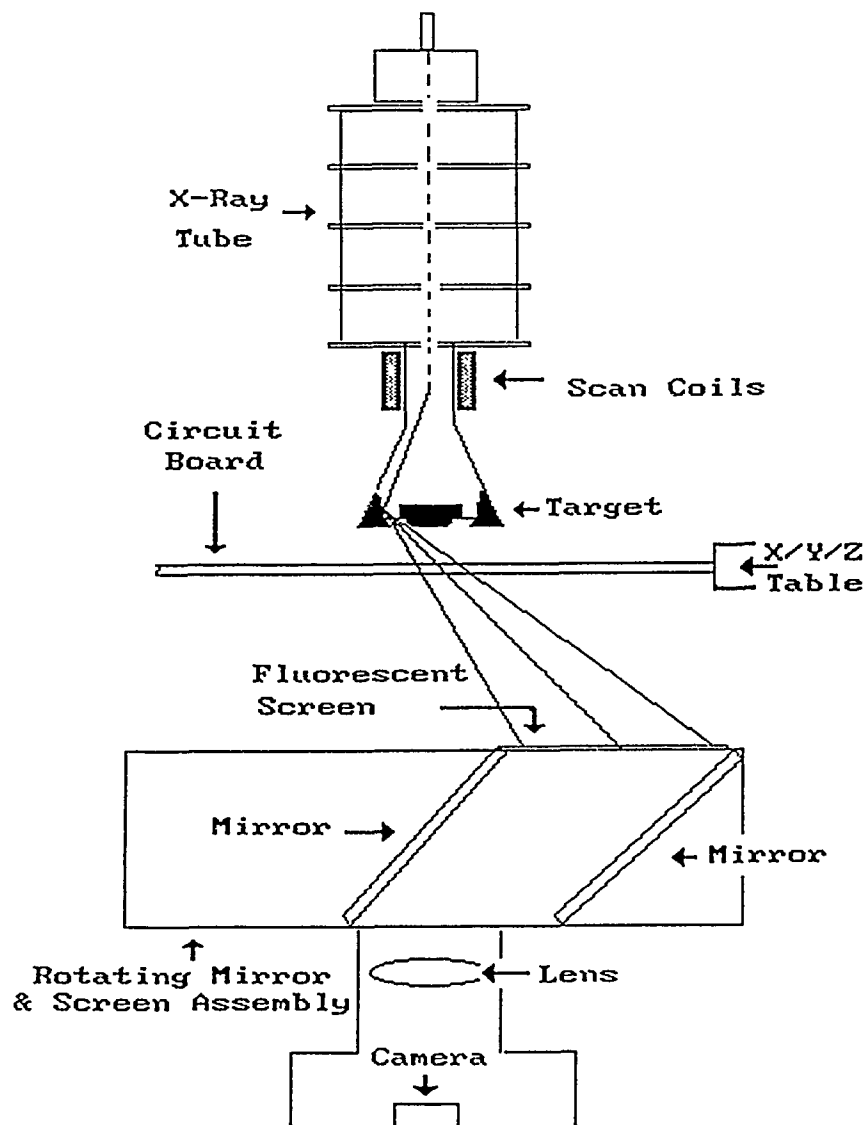
FIGURE 5. Scanned-Beam Laminography.

THE NEW SCANNED-BEAMED LAMINOGRAPHY

The Scanned-Beam Laminography System scans the electron beam within the X-ray tube causing it to follow a circular path on the X-ray target within the tube. The electron beam is synchronized to the rotating detector. The X-ray image falls onto the detector screen and is converted to a visible image by the screen. The mirrors within the rotating detector de-rotate the image and allow the fixed low-light level camera to view the image. The video signal is digitized into a computer system. The laminographic image is generated by integrating the resulting image for one trip around. The detector spins at 600 RPM so a laminographic slice is generated in 100 milliseconds.

In the inspection of circuit boards, the boards are mounted on an XYZ table. The area to be examined is moved into view, and the Z-axis moves the board up and down through the Z-focus plane to select where in Z on the board the slice is to be taken.

SELECTED IMAGE COMPARISONS

In the following section, images of through-hole and surface mount devices are shown for both conventional X-ray and Scanned-Beam Laminography.

Figure 6a shows an X-ray of a through-hole connector with internal voiding. Figure 6b gives a line plot of the gray-scale signal of the void.

Figure 7a shows a laminograph of a through-hole connector at the level of the internal voiding. Figure 7b gives a line plot of the gray-scale signal of the void. The laminograph presents a much clearer signal to analyze than that shown in Figure 6.

Figure 8 shows an X-ray image of a J-lead component with bridging between leads.

Figure 9 shows the laminograph of the same device as in Figure 8; however, notice how the "noise" from the surrounding lead and package material basically disappears in the laminograph.

Finally, if slices are taken at closely spaced intervals, a 3-dimensional reconstruction of the solder joint is possible. Figure 10 shows such a reconstruction.

FIGURE 6a. X-Ray of Through-Hole Connector with Internal Voiding.

FIGURE 6b. Line Plot of the Gray-Scale Signal of the Void.
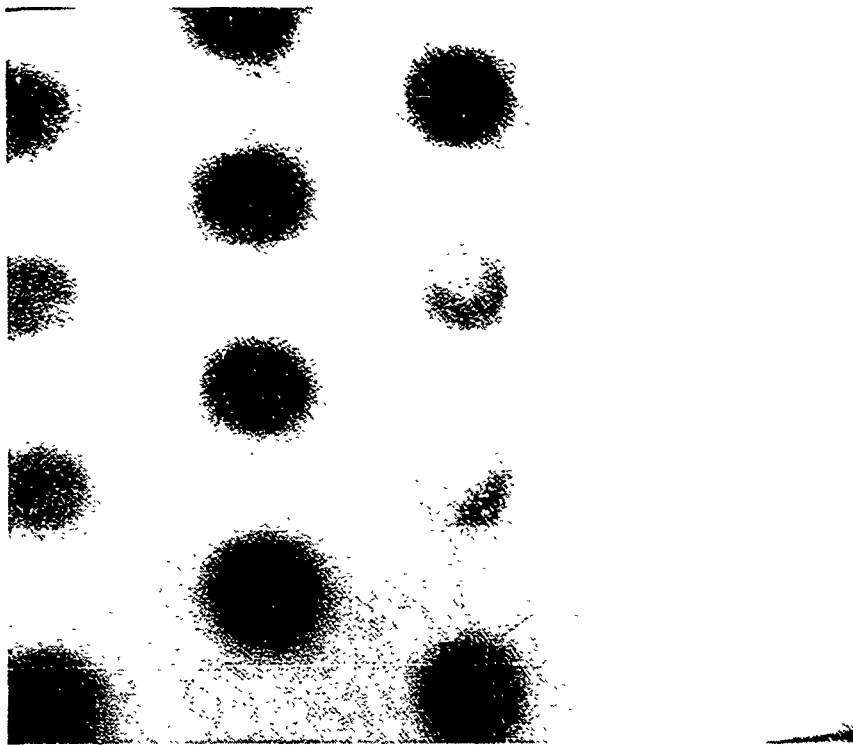
FIGURE 7a. Laminograph of Through-Hole Connector at Internal Void Level
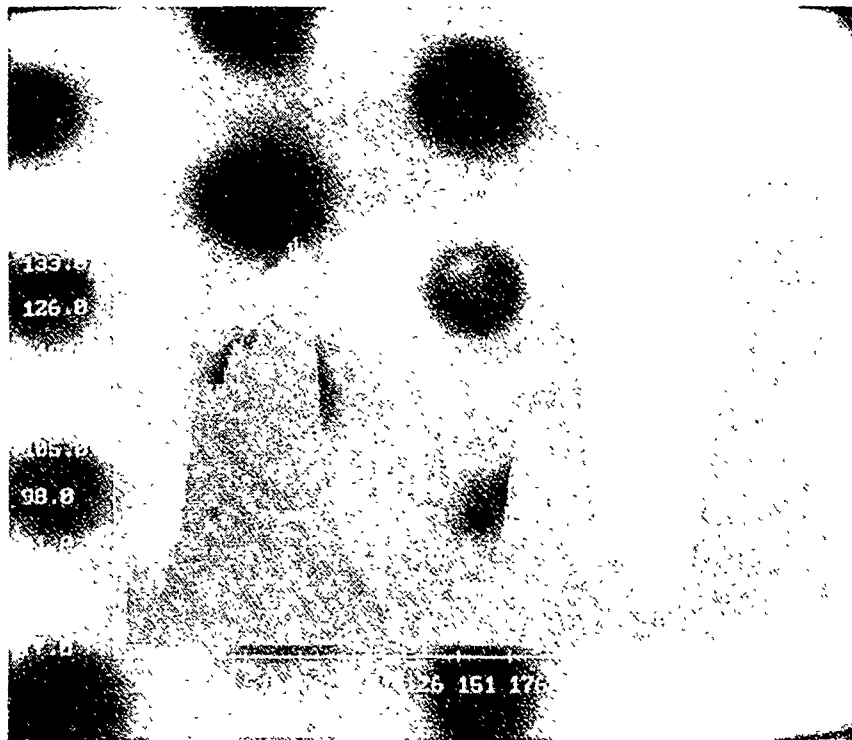
FIGURE 7b. Line Plot of the Gray-Scale Signal of the Void.
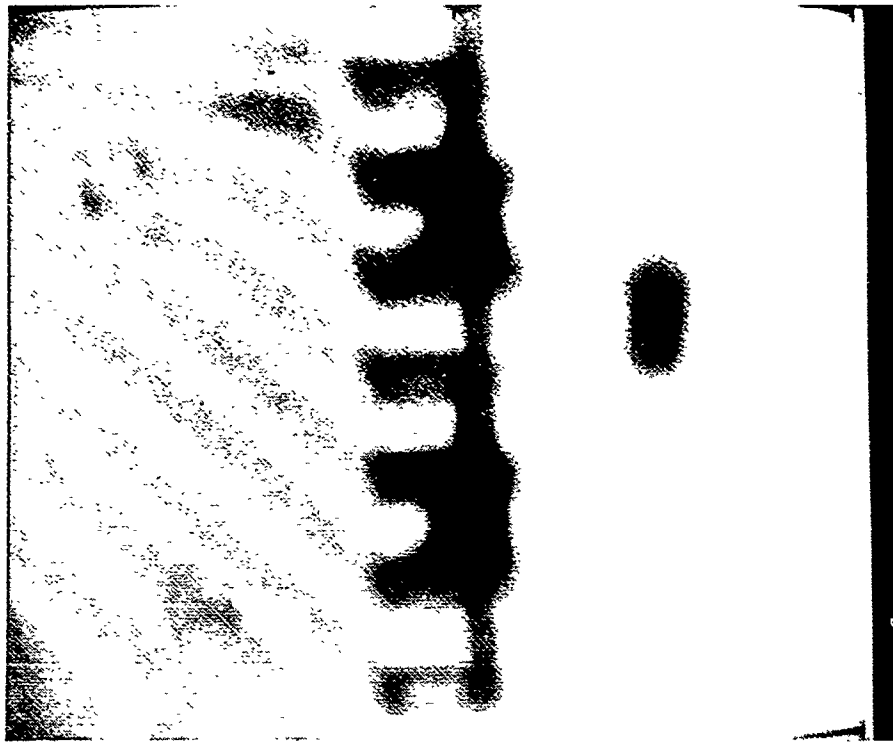
FIGURE 8. X-Ray of J-Lead Component with Bridging Between Leads.
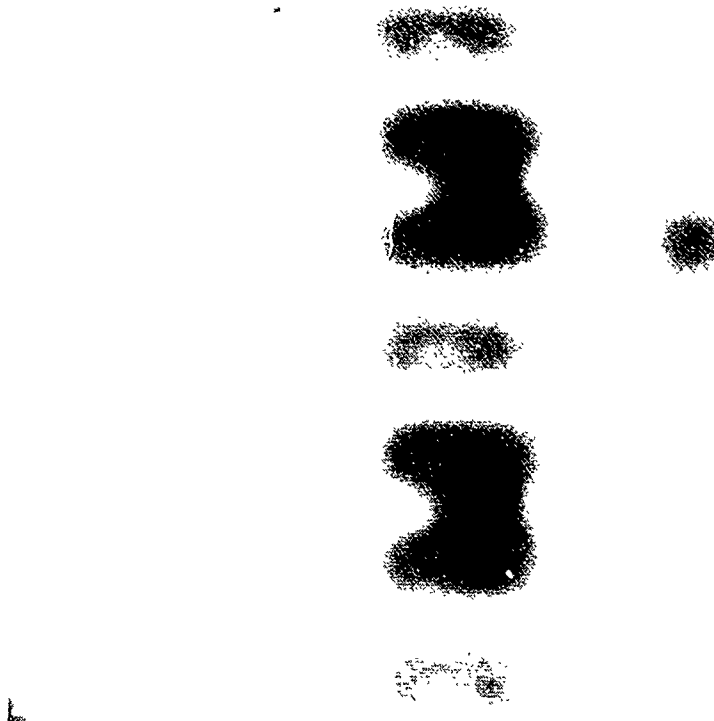
FIGURE 9. Laminograph of J-Lead Component with Bridging Between Leads.
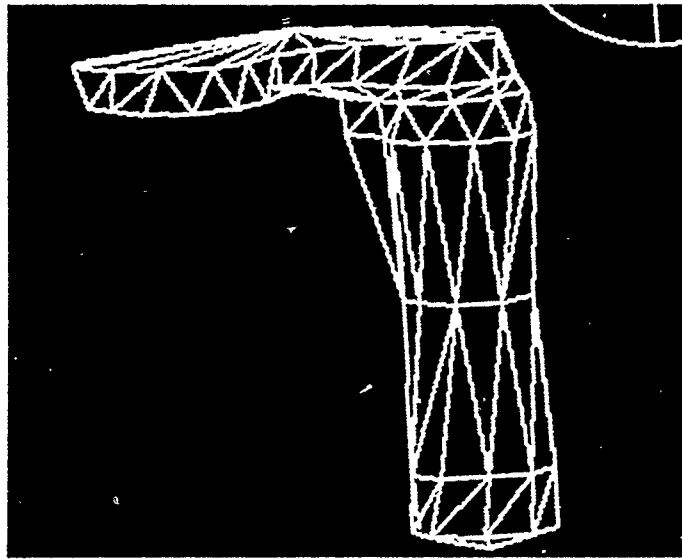
FIGURE 10. 3-Dimensional Reconstruction of Solder Joint

SUMMARY

Visual inspection of boards for solder quality is extremely difficult and critically dependent upon the viewer's interpretation of solder quality specifications and the individual's fatigue level. Solder joints are frequently obscured from view, and internal defects are not found. The ever increasing density of solder joints requires increased magnification and lengthens the time taken to inspect a board.

Most solder joint anomalies are ideally suited to inspection by Scanned-Beam Laminography. These include bent or missing leads, insufficient solder, solder balls, and bridging between components. Two-dimensional X-ray images do not have the capability of fully examining double-sided SMT boards. The three-dimensional information provided by Scanned-Beam Laminography simplifies image analysis.

Scanned-Beam Laminography data is also ideal for generation of process control data. Amount of solder, distribution of solder, and pad-to-pin alignment are but a few of the possible process parameters that SBL can reliably measure.

Since Scanned-Beam Laminography relies on slicing in the Z-axis, simple X, Y data from a CAD system should allow automatic programming of an inspection system.

Scanned-Beam Laminography holds great promise for industry wide use for the inspection of soldered connections and for monitoring the process.

REFERENCES

1. John Adams, "Process Control in SMT Soldering," *Surface Mount Technology*, October 1988.

2. T.D. Doan, "Infra-Red Technology for Automated Inspection of Lap Solder Joint," Naval Weapons Center, China Lake, CA, February 1987. NWC TP 6789, 11th Annual Electronics Manufacturing Seminar Proceedings.

3. Douglas H. Ensign, "Laser Inspection Calibration Baseline for Thermal Signature Analysis," Naval Weapons Center, China Lake, CA, February 1987. NWC TP 6789, 11th Annual Electronics Manufacturing Seminar Proceedings.

4. M.P. Seah and C. Lea, "Certainty of Measurement using an Automated InfraRed Laser Inspection Instrument for PCB Solder Joint Integrity," *Journal Phys. E:Sci.Instrum*, Vol. 18 (1985), pp 676.

5. Patrick E. Casey, "X-RAY Inspection," *Manufacturing Systems*, July 1987.

6. Edward W. Soron, "X-Ray Inspection Meets Increased PWB Throughput, Density Challenge- Part 1." *Electri•onic Electronic Edition*, October 1987.

7. Lawrence Kessler, "Testing Lead Bonds in VLSIC Devices by Acoustic Microscopy,"*Test & Measurement World*, Jan 1986.

8. Charles D. Goodwin and Galen J. Reader, " Real-Time X-ray Process Control For Solder Joint Integrity," June 1987. Proceedings of the Technical Program, NEPCON East 1987, Boston, MA.

9. Thomas S. Curry III, et al., " Christensen's Introduction to the Physics of Diagnostic Radiology," 1984, 3rd Edition, Chapter 24. Lea & Febiger, ISBN 0-8121-0918-X.

10. A.E.M. Bocage, French Patent 536464 (1922).

11. F. Protes and M. Chausse, French Patent 541941 (1922).

12. E. Pohl, Imperial German Patent 544200 (1927-1932).

13. Thomas S. Curry III, et al., "Christensen's Introduction to the Physics of Diagnostic Radiology," 1984, 3rd Edition, Chapter 18. Lea & Febiger, ISBN 0-8121-0918-X.

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AUTOMATED SOLDER JOINT INSPECTION IN A CCAPS ENVIRONMENT

by

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ABSTRACT

In the Circuit Card Assembly and Processing System(CCAPS) program, a feasibility study was done to demonstrate inspection of Solder Joints on card assemblies by Machine Vision. It is possible to not only detect defects, but to correlate them to definitized shape parameters. It is inferred from this study that Machine inspection is superior to Human inspection. CCAPS is poised to take advantage of these technologies, namely, 3D and 2D Vision, and 3D Xray.

INTRODUCTION

Building Quality Into The Process

In today's environment, where productivity is a key contributor to the business health of the nation, every labor hour we save is important to the overall cost and quality of our product. Given those conditions, it is imperative that Solder Joint Inspection has as key a role as any other manufacturing process. Although, inspection is not a value-add process, it is a necessary requirement for outgoing product quality.

The traditional methods of Solder Joint inspection have been one of dependency on Human Inspectors. The "Eye-Ball" technique has serious disadvantages. Human errors, due to strained eyes, clerical errors, incorrect touch-ups and re-training for newer people are the main disadvantages.

Automated Inspection, which is basically by machine-systems, eliminates the disadvantages of human inspection. Machine-systems are hard to teach, but once taught, they are steadfast in the rules created in them. There are no judgement calls, but strictly rules based.

In the area of Circuit Card Assembly and Processing (CCAPS), IBM has been examining the areas of automation; inspection stood out as a very good candidate for automation. This offers the advantages of automated feedback, reduced rework, pinpointed touchups, and elimination of human labor.

Triple technology inspection was chosen, based on a feasibility study, described later on in this paper. The three technologies selected constituted : 3D Vi-ion, 2D Vision and Xray. 3D Vision looks at Topographic Defects, 2D Vision looks at Surfac.. or Color Defects and Xray looks at Internal Defects.

This kind of system will provide a complete inspection of all the 24 solder joint defects and has the potential to provide process feedback. The process feedback would be in the areas of : (a) Incoming Inspection, (b) Reflow characteristics (c) Solder application process and (d) an Overall Quality Report Card on the health of the card assembly process.

If 2D Vision and 3D Vision systems are merged into a single machine, a separate machine can be created for Xray inspection. The Xray system would be a 3D Xray system, doing laminography inspection of solder joints. Together , these two systems would provide the triple technology inspection that was discussed above. The 3D Vision system would customize shape criteria thru First Run Articles. An example would be the inspection of solder joints having either Bulbous or Non-Bulbous Joints. Similarly, an Xray system, with adequate software program, would distinguish between many criteria in the solder joint and its external surroundings. For example, buried copper planes can be filtered in a 3D Xray environment.

THE FEASIBILITY STUDY

In September'86, IBM subcontracted the Feasibility Study to RVSI, a machine vision company in Long Island, NY. The requirements of the study were to demonstrate that Automated Inspection was technically feasible and machines could replace the human inspection process. In addition, RVSI had the responsibility to investigate all the machine inspection capabilities in the areas of 3D Vision, 2D Vision and 2D Xray. They had to judge the above three technologies in the areas of 24 Defects , against samples of LCCs, Flatpacks and Thru Hole components.

The list of defects were assigned responsibilities for detection under the three technologies, per Figure 1. Notice how the line of sight defects were assigned to 3D Vision and 2D Vision and defects internal to the joints were assigned to Xray.

DEFECT	DETECTION CAPABILITY		
	2-D	3-D	X-RAY
BRIDGING	★	★∕	★∕
BURNED OR HEAT DAMAGED	●∕		
COLD SOLDER JOINT	.	★∕	
CONTAMINATION	●∕	□	□∕
DEWETTING	□	★∕	
EXCESS SOLDER	□	★∕	●∕
FRACTURED OR DISTURBED CONNECTION	●∕	◉∕	□
GRAINY SOLDER	●∕	●∕	
INSUFFICIENT ELECTRICAL CLEARANCE	●	★∕	★∕
INSUFFICIENT SOLDER	□	★∕	★∕
INTERNAL VOIDS			★∕
LACK OF SOLDER COVERAGE ON LEAD ENDS	●∕	●∕	●

DEFECT	DETECTION CAPABILITY		
	2-D	3-D	X-RAY
NONREFLOW		★∕	●
NONSOLDERED CONNECTION		★∕	●∕
OVERHEATED SOLDER	●∕	□	
PITS, HOLES OR SURF. VOIDS	□	★∕	●
POOR WETTING		★∕	□
ROSIN CONNECTION	★∕		□
SOLDER IN BEND RADIUS	□	◉∕	□
SOLDER NOT SMOOTH AND SHINY	★∕	●	
SOLDER POINTS, PEAKS AND ICICLES	□	★∕	●
SOLDER SHRINKAGE	●	●∕	
SOLDER SPLATTERING	●	●∕	★∕
STRESS MARKS	●	●∕	

★ CAPABLE   ● SOMEWHAT CAPABLE   □ MARGINALLY CAPABLE   ⊿ RESPONSIBLE TO DEFECT

Fig.1: Capabilities & Responsibilities of Three Technologies

The Details Of The Study

The study requirements were defined such that 3D Vision would be a developmental study, involving hardware and software approaches that had not been tried before. For example, the 3D Vision portion of the study would adopt a Dimensional approach to solder joint Pass/Fail Criteria. The dimensional approach is analogous to a river valley's dam design. To elaborate, in the design of such a dam, the ratio of base length to the height of the dam is part of a given structural strength design. Similarly, in solder joint strength assessment, there would be a certain height, base length, slope, and volume as part of the strength requirements. Conceptually, each solder joint is a mechanical structure.

Dimensional approach utilizes these principles of solder joint formation . The 3D Vision software development hinged on this principle. Since such numerical data was not readily available, defects of varying intensity were created in each of the 24 defect categories.

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In the 3D Vision area, RVSI took each of the solder joint samples and inserted them in a bread-board setup. The structured light laser technique used in this breadboard gave a feedback to the camera on the exact x,y,z position of the spot on which the laser impinged. Using very fine resolutions, the laser looks at a multitude of points on a single solder joint. All these points, when collected and stored in a computer memory, constitute Raw or Preprocessing Data. Figure 2 shows the laser impingement on a solder joint (Flatpack).
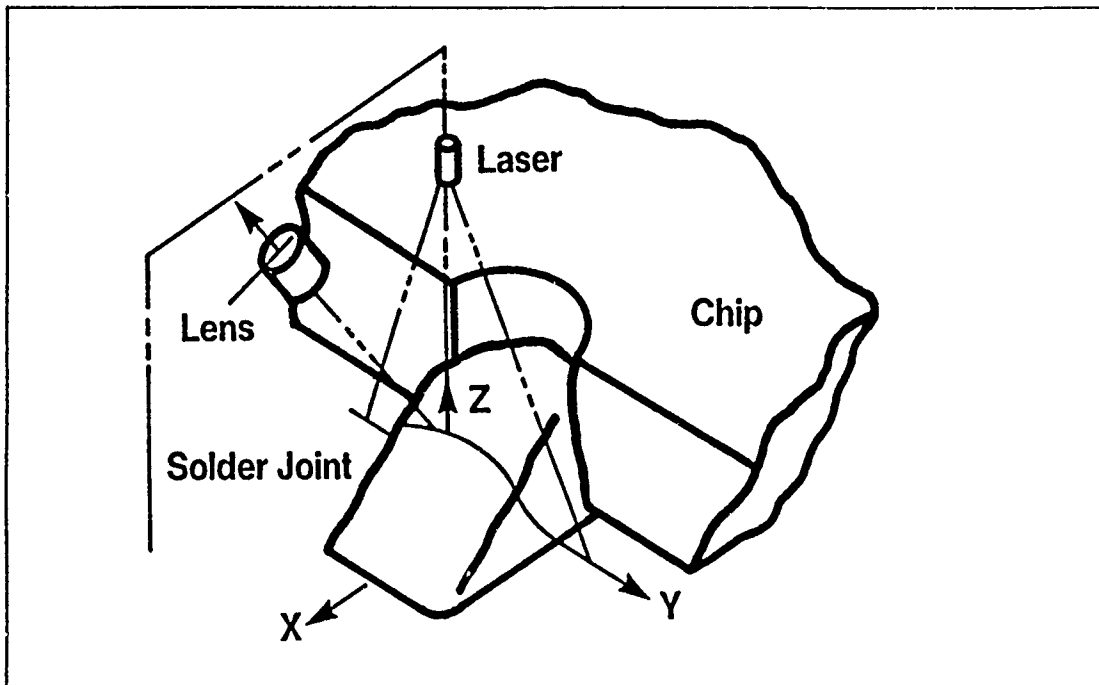
Fig.2: 3-D Machine Vision Technique

Using a series of software algorithms, per Figure 3, the Data is processed to higher and higher levels of human understanding The series of steps starts with Segmentation and ends with Defect detection. Each of the software steps is modular.

The final stage in the Software algorithm steps is "Defect Detection". As shown in Figure 4, the list of possible defects within a single joint is shown with certainties or probabilities. The highest probability of a single defect category occuring within a joint is 1.0 , and the lowest is 0.0. Taking a 0.35 as a reasonable probability of occurence, Figure 4 shows this particular flatpack joint to have "Excessive Solder" and 'Dewet" as two highly probable defects on this joint. Manual verification proved this to be true.
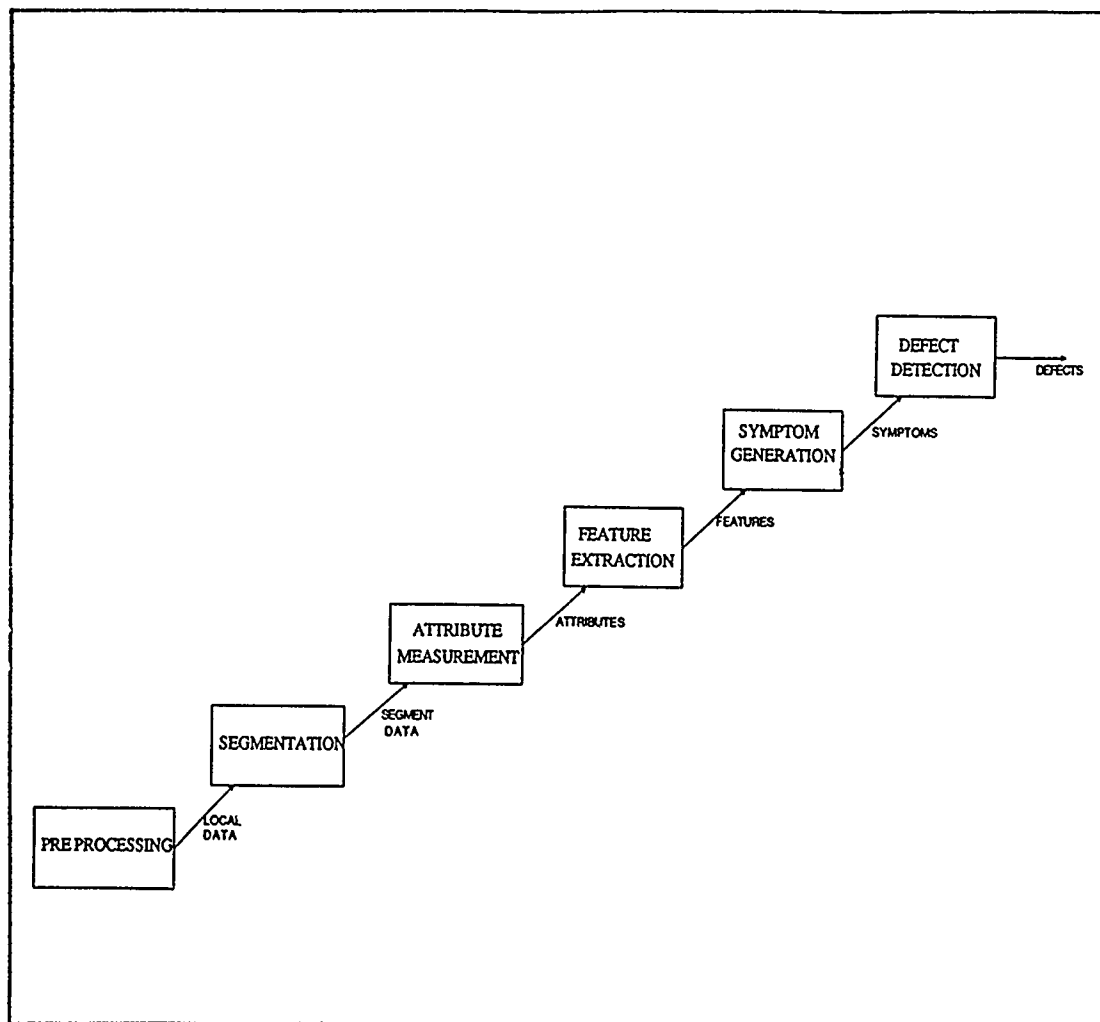
Fig.3: 3-D Inspection Data Flow

```
Bridging                          : 0.250000
Insufficient Elec. Clearance : 0.250000
Cold Joint                        : 0.190000
Dewet                             : 0.625000
Excessive Solder                  : 0.812500
Fractured                         : 0.000000
Grainy                            : 0.000000
Insufficient Solder               : 0.000000
Lack of Solder on Lead End   : 0.000000
Non-Reflow                        : 0.000000
Not Soldered                      : 0.000000
Pits or Holes                     : 0.000000
Poor Wetting                      : 0.190000
Solder in Bend Radius             : 0.000000
Peaks or Icicles                  : 0.000000
Splatter                          : 0.000000
Solder Shrinkage                  : 0.000000
Stress Marks                      : 0.000000
Missing Lead                      : 0.000000
Unidentifable Defect              : 0.000000
```

Fig.4: FP Defect Certainties, FP Joint #7

In the next series of figures, several flatpack joints are shown both in the raw data format, where x,y,z plots are shown, and in an outer dimension profile. For example, Figure 5 shows the surface topography of a Good Flatpack Joint, while Figure 6 shows the average outside dimensions of the same joint. The latter dimensions help in measuring, if necessary, the criteria for a good joint. Similarly, Figure 7 shows the topography for an excessive joint, while Figure 8 shows its outside dimensions. Figure 9 shows the topography of an insufficient joint. Notice how the lack of x,y,z dots in select areas show up. These would be the areas lacking solder. In Figure 10, the outer dimensions plot go to prove this point.
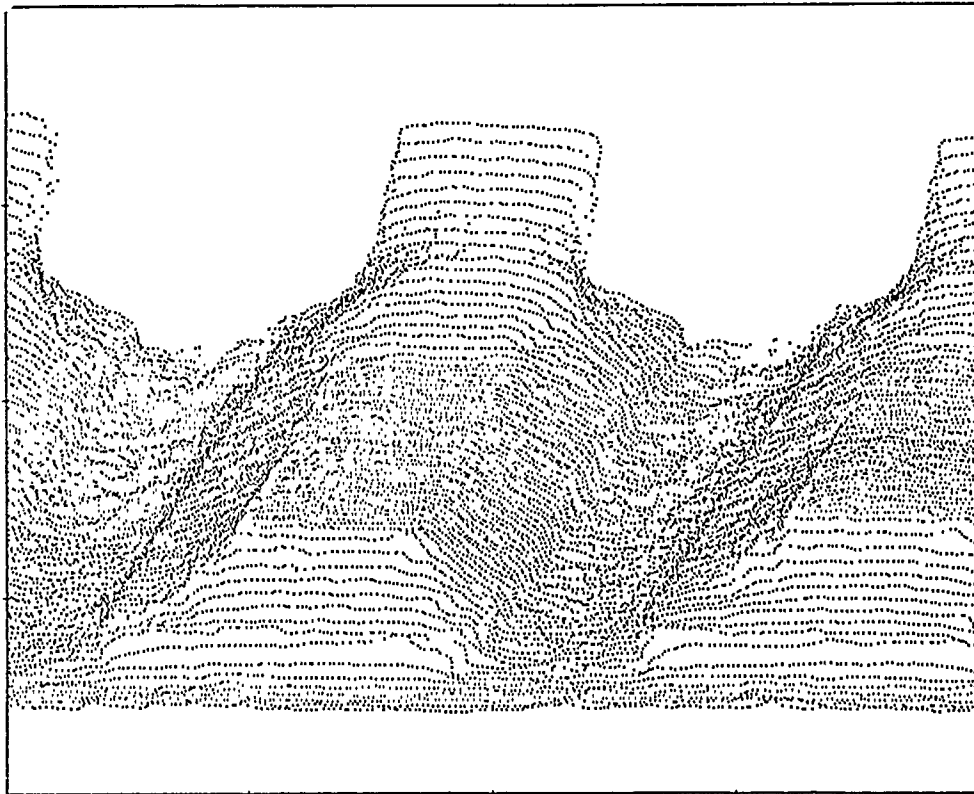
Fig.5: Good Flatpack Joint

Fig.6: Local Data for a Good FP Joint(Basis for Segmentation Software)
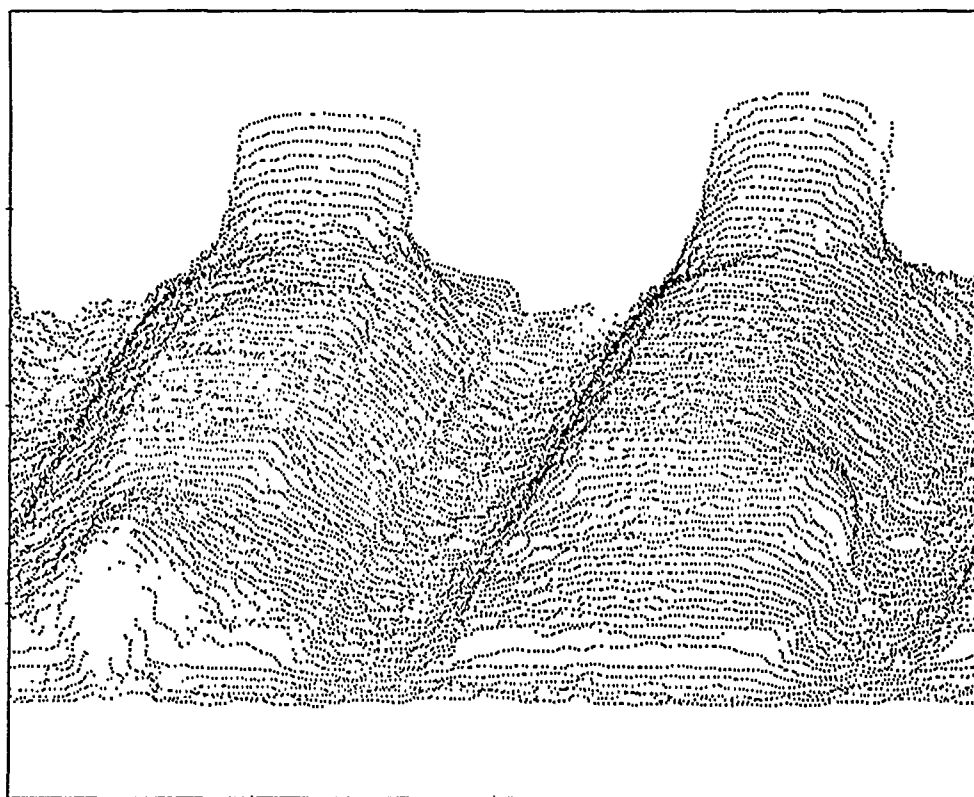
Fig.7: Excessive Solder On Flatpack Joints
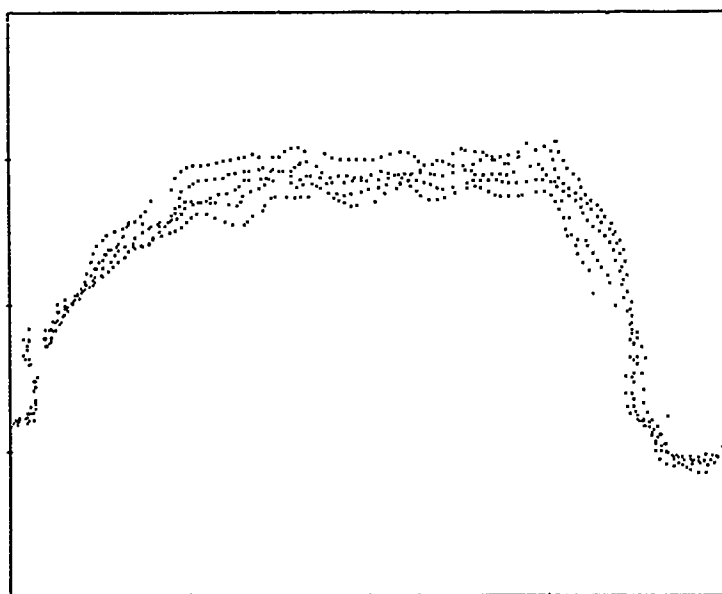
Fig.8: Cross-Section of FP Joint (Excessive Solder)
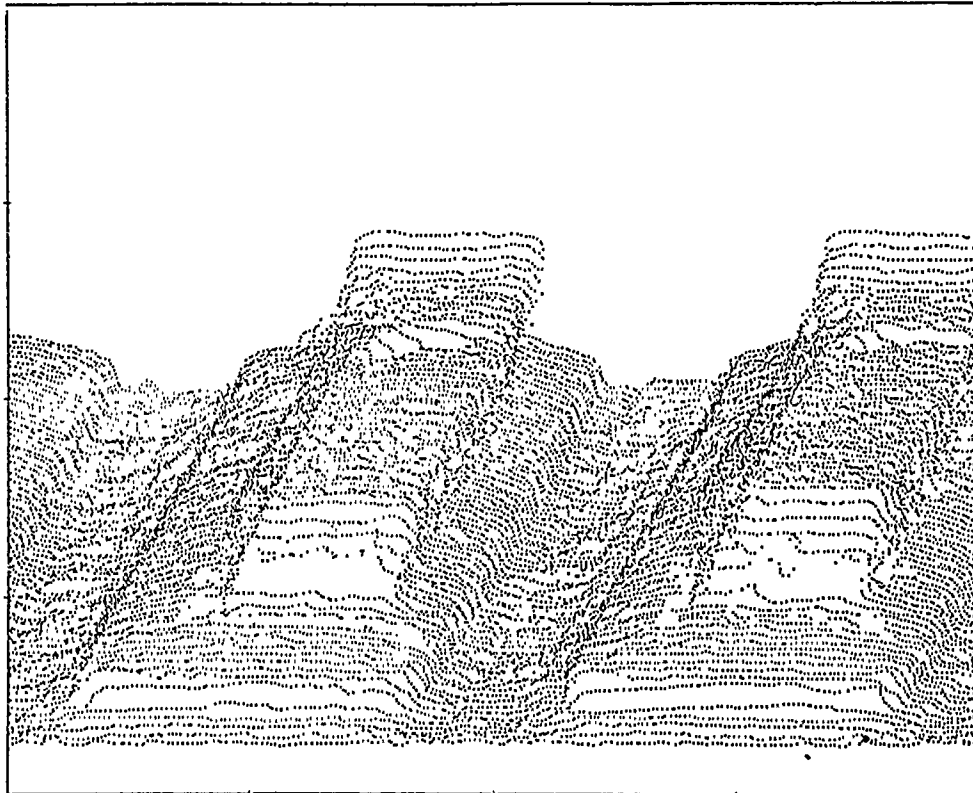
Fig.9: Insufficient Solder On Flatpack Joints
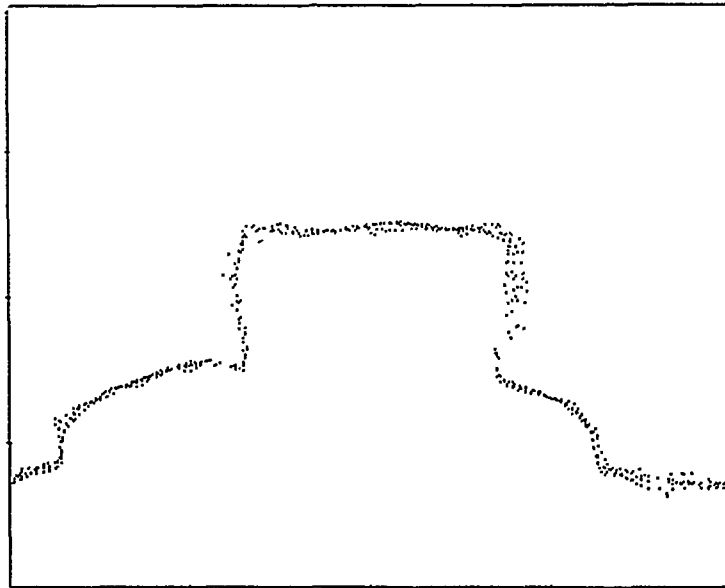
Fig.10: Cross-Section of Flatpack Joints (Insufficient Solder)

The 3D Vision system also looked into LCC solder joints and Figure 11 depicts a sideview of datapoints of an LCC castellation, filled with solder and attached to the board. Notice how the topography changes with the amount of solder, both in the lower attachment area and the upper castellation area. The second joint from the left is starved of solder in the middle region. The 3D Vision system also measures the net dimensions required for a good solder joint, including the width of the castellation, the total height of the joint along the LCC wall and gives a summary report on each joint's status.
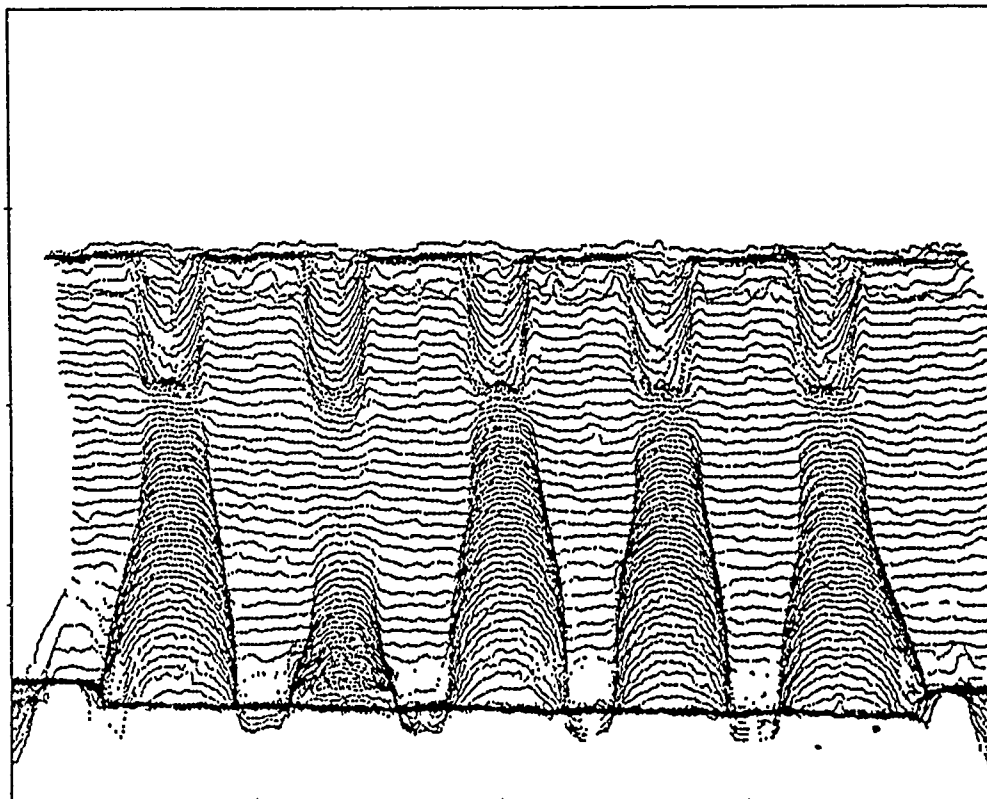
Fig.11: LCC Joints (Viewing Castellations, sideview)

Figures 12 and 13 dramatize the difference between the way an inspector looks at LCC joints and the way a machine looks at them. In Figure 12, for example, an inspector looks at the very joints and does a comparative judgement. The inspector looks at the solder joint and compares with the castellation width. The solder joint is perceived as ACCEPTABLE. However, the machine had been taught the basic dimensions of a good joint and "measures" these strictly without applying any judgement. The machine's call of EXCESSIVE was verified as correct. Similarly, the opposite effect took place in Figure 13.
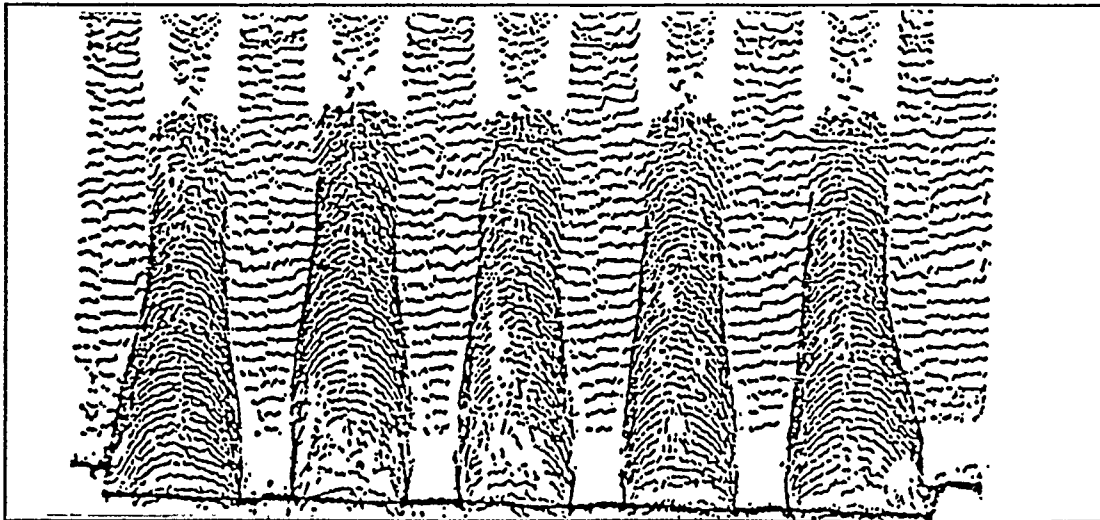
Fig.12: LCCs (Human Inspector = Acceptable, 3-D Vision = Excessive)
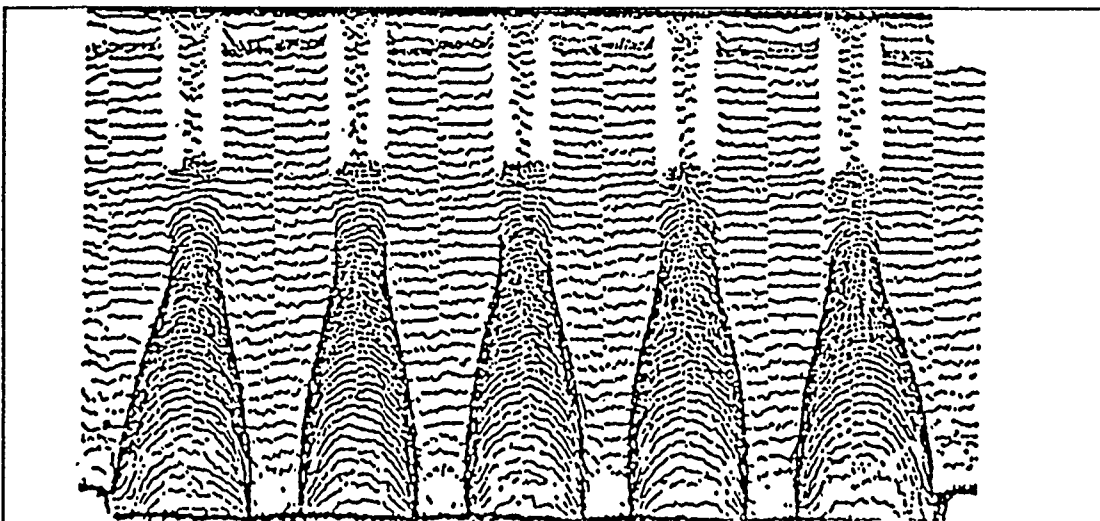
Fig.13: LCCs (Human Inspector = Excessive, 3-D Vision = Acceptable)

Each joint is also depictable from a profile perspective. Figures 14, 15 and 16 show the average curvature of a solder joint shape as it fills the LCC castellation. The LCC component's vertical wall is shown as a dotted line. The board's horizontal surface is also shown as a dotted line. Notice how the 3D Vision's profile view provides the ability to measure the level of solder along the castellation height (the mid-point of the castellation height is the key criteria);and, secondly the gap between the component and the board surface. Each of these would be an inspection measurement. It is difficult for the human eye to view these differences thru a microscope.
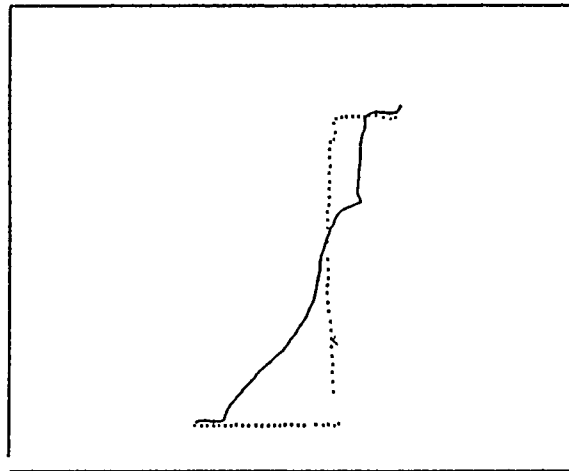
Fig.14: LCC Sidewall (dotted line) and Solder Profile (thin line)
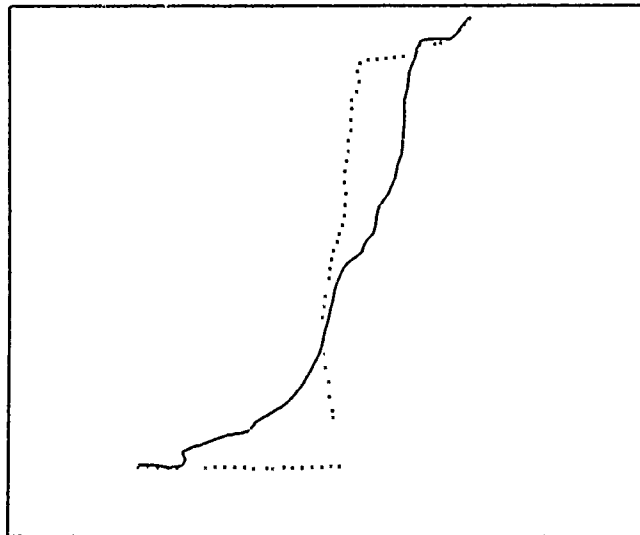
Fig.15: Solder Profile Below the Castellation Mid-Point in LCC
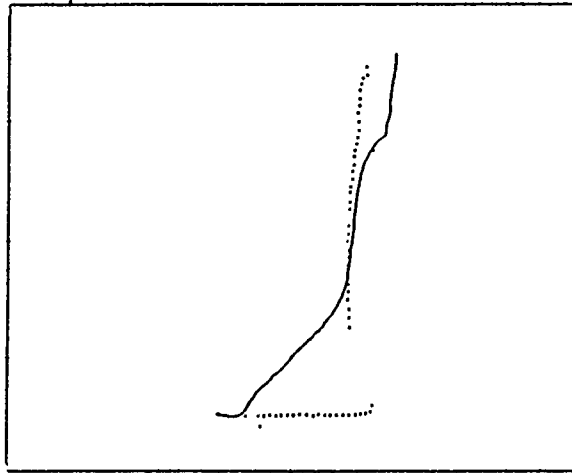
Fig.16: LCC (vertical dotted line) OFF the Board Surface
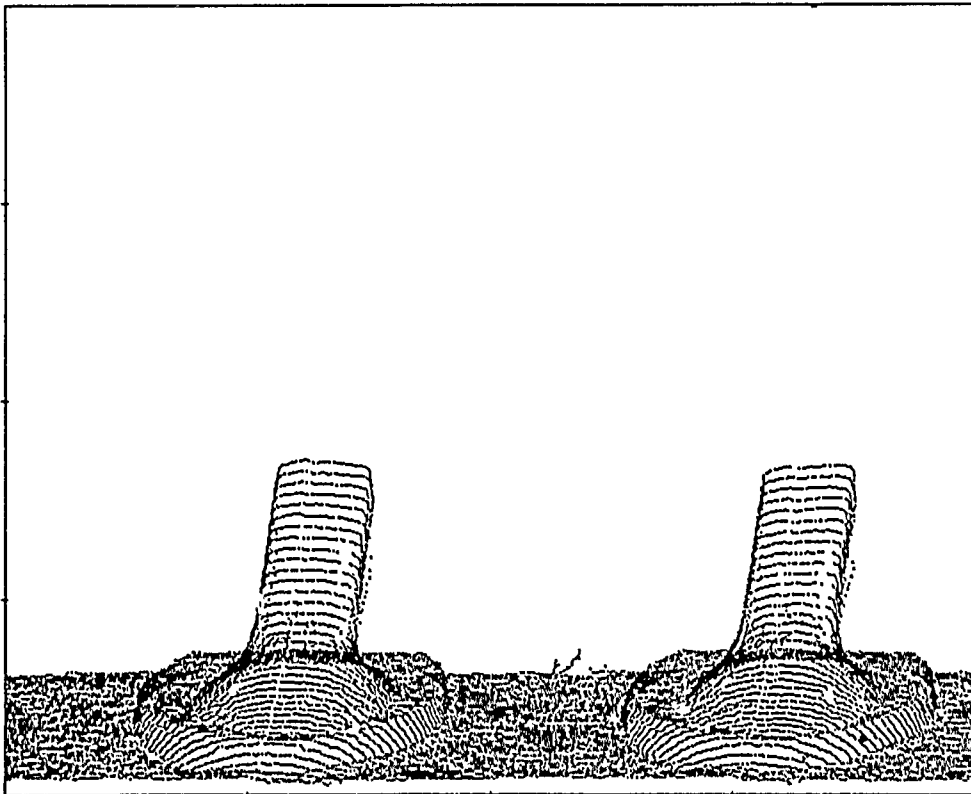
Fig.17: DIP Joints (Good Joints)
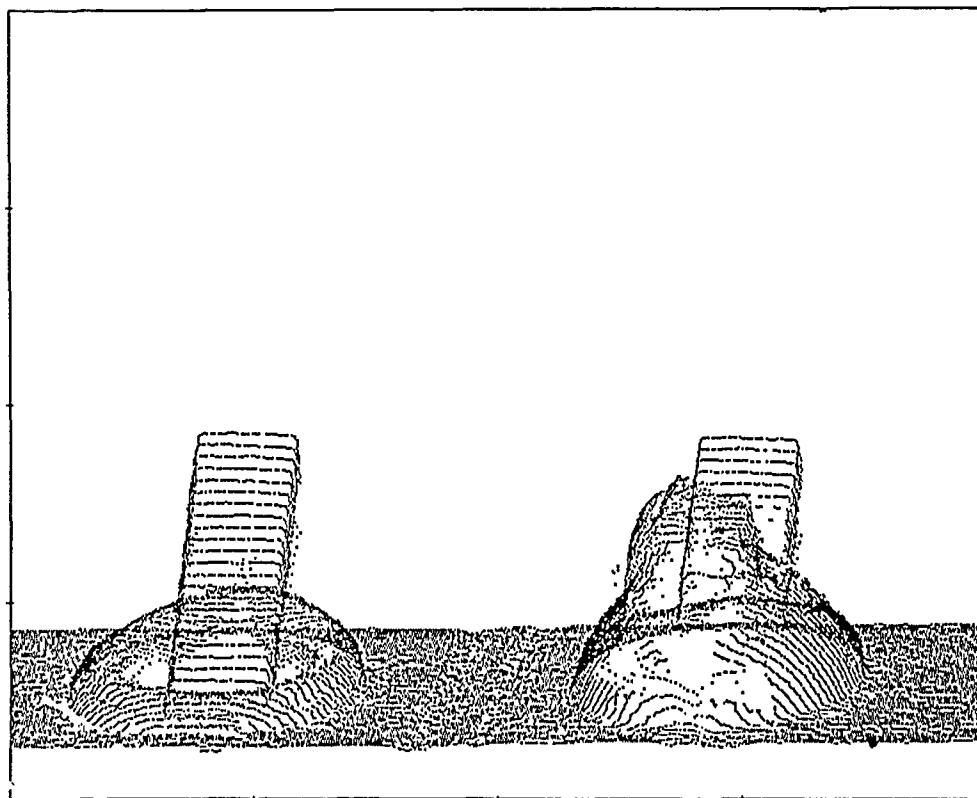
Fig.18: DIP Joints (Non-wetting (Left), Peak (Right))

In the areas of thru-hole inspection, the 3D Vision system can differentiate between good joints and bad joints as shown in Figures 17 and 18, respectively. The bottom side of a DIP joint is topographically mapped and the figures show evidence of "non-wetting" (absence of solder) and "peak".

RESULTS OF STUDY

The study concentrated in the areas of 3D Vision development, primarily, but also looked at the feasibility of 2D Vision and 2D Xray. The objective of this study was to achieve a high success rate in each of the three technologies that were being looked at for a final inspection system. From that perspective, the study showed complete success. Figure 19 shows the Success Rate.

SUCCESS RATE = 100% - (ESCAPE RATE + FALSE ALARM RATE)

Escape Rate can be defined as the percentage of defects escaping detection and going into the field. False Alarm Rate can be defined as the percentage of good joints that give an apparent "defect" in the inspection system. During the blind test, unmarked defects were tested for system validity. Machine inspection calls were tested against manual inspection.

The results of this study showed that each of the technologies was independently feasible. The study also pointed out some of the specific tasks that each of these technologies can do. For example, 2D Vision can look at surface discoloration and contamination defects. Xray can look at internal voids. Based on these qualitative findings, it was decided that in a two-system workcell approach, the best strategy would be to have 3D and 2D Vision systems incorporated as a single system. This would be the first system in the workcell. The second system would be the Xray system. Both of these make up the total workcell for Automated Inspection. Identification of internal defects and masking of the environmental features were important in an Xray inspection system, especially with buried copper planes within the board. It was decided that a Laminographic Xray system would be best suited for this application. The ultimate CCAPS system design would be a two-system workcell: a Line-of-Sight Defect Detection System and an Internal-to-the-Joint Defect Detection System.

This strategy would cover the complete inspection requirements of solder joints. At the same time, an automated system would be responsive to the changing partnumber sequences in a CCAPS production area, where partnumber data can be downloaded into the workcell. The component type,location and the unique characteristics of each joint would be part of this partnumber data. Automated Inspection, which eliminates operator involvement, gives rapid, realtime feedback to the soldering processes. In the future, Automated Inspection can be broadened to inspect non-solder characteristics, such as board warpage, incoming raw material quality, and a complete outgoing inspection of the overall production process.

SUCCESS RATE

100%
90   94   83

50%

ESCAPE RATE

50%
5   4   7

FALSE ALARM RATE

50%
5   2   10

3-D   X-RAY   2-D
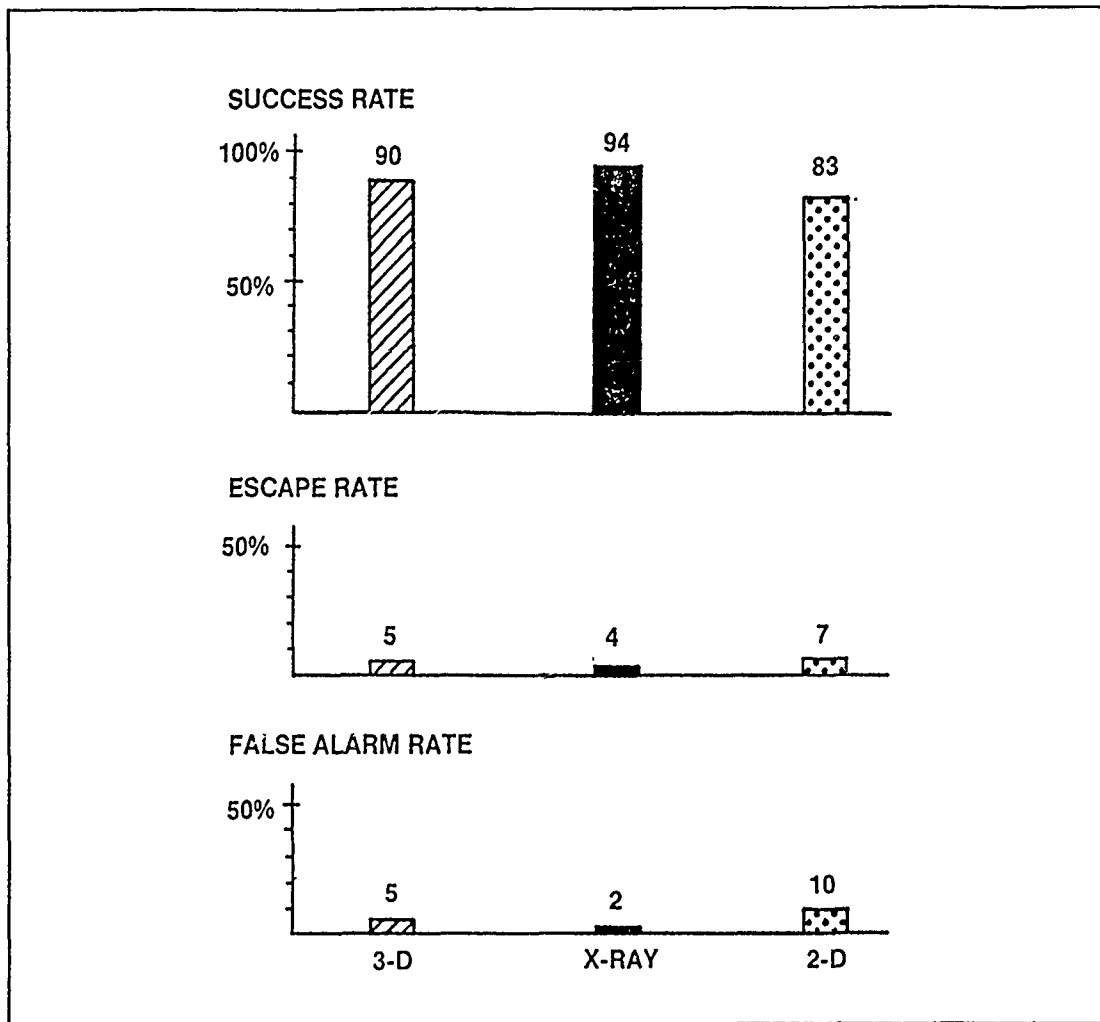
Fig. 19: Final Test Results of Study

CONCLUSIONS

One of CCAPS' goals was to develop and build automated card assembly systems. In pursuit of this goal, a feasibility study was undertaken to examine the three technologies in inspection. The study demonstrated a high success rate for the 3D Vision, 2D Vision and the 2D Xray technologies. The study concentrated on developing a practical tool in the 3D Machine Vision area. The paper shows in detail the topographic effects of 3D Vision and its applications in a production environment. The paper goes on to establish a viable workcell which comprises of a 3D Vision system (all Surface Defects) and Laminographic Xray system (all Internal Defects). Automated Inspection can eliminate strained Human Inspection and provide realtime process feedback to the production process.

In the areas of inspector inconsistencies, there are two subdivisions. Firstly, a single inspector can look at a very joint, repeatedly, after elapses of time, and make a different inspection call everytime of either "good" or "bad" joints, or in terms of differing defect classifications. Secondly, different inspectors looking at the same joint can give differing calls both in terms of Pass/Fail and defect classification.

Machine-Vision is consistent, and makes the same calls day in and day out. If there is one weakness with Machine-Vision, it is that it has been taught its Inspection Criteria on the basis of Human Standards. The Dimension Criteria is a step towards scientific calculations of Solder Joint strengths.

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Durability Test Development

From Design Duty Cycle Determination to Test Profile
Development

Michelle Lindsley

ABSTRACT

Durability as a measurable, testable figure of merit
for electronics was initiated by the Air Force's
Aeronautical Systems Division's Avionics Integrity Program
(AVIP) in the mid 1980's. The durability test is used to
verify that the electronic system can operate, without
failure, throughout its intended lifetime of time varying
environmental stresses. The basis of the durability test
profile is the design duty cycle. The design duty cycle
incorporates the life cycle environmental exposure of a
particular electronic system with its designed operational
configurations. To outline the process for durability test
development, a case study is presented on developing the
design duty cycle and durability test profile for a
communications black box on a modern fighter aircraft.

INTRODUCTION

Durability testing is another form of reliability life
testing. To simulate a lifetime of low and high cycle
fatigue as encountered in operation, the design duty cycle
is used as the basis for the durability test profile. The
design duty cycle is composed of environmental and
operational situations the product is likely to encounter
during its intended lifetime. The durability test profile
exposes the electronic system to a lifetime of environmental
stresses, including power on/off cycles. Environmental
stresses and power on/off cycles lead to low and high cycle
fatigue of interconnections such as solder in electronic
assemblies.

This paper starts by defining each life cycle
environmental event for a communications black box. Next it
shows how to determine the design duty cycle for each life
cycle event with suggestions for test parameter development
and suggested approaches for test time compression and/or
acceleration. It ends with a method for the durability test
flow. Presently, the environmental data base necessary to
develop any type of environmental test profile does not
exist to the level necessary for the overall design of

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military and commercial sophisticated hardware. However, the process outlined below uses currently available environmental data for a first order approximation in developing the durability test profile theory.

LIFE CYCLE ENVIRONMENTAL CHARACTERIZATION

For this case study the life cycle situations a communications electronic device used on a modern fighter aircraft is likely to encounter, after its release from manufacturing, include: transportation from manufacturing to storage to use, extended storage, mission use and maintenance. Since the primary objective of a durability test is to simulate low and high cycle fatigue (repeated stresses), temperature and dynamic environments are considered for this application. (For realism, corrosive environments must also be considered because of the introduction of chemical failure mechanisms during long term storage or after long term exposure to corrosive environments- but simulation of corrosive environments is not addressed here due to limitations in the scope of this paper). However, to environmentally qualify an electronic system the following environments should also be considered depending upon the application, storage and deployment locations: rain, icing, snow, moisture/humidity, sand, dirt and dust, salt fog (and other corrosive environments), acceleration and altitude.

One way to start on the life cycle characterization, is with an Life Cycle Events versus Environments Matrix (Figure 1). To start the Matrix, first identify data you have, then identify data you know exists, and finally identify the areas where you don't have data and where you're not sure if it exists. Figure 1 already lists the data sources in the boxes -however, as mentioned above, most data are not exact and only a first order approximation.

Event/ Environments		Trans.	Storage	Mission Use	Maint.
Temperature	Hot	UPS	Ref. 1	ASIP/210	Repair Tec.
	Cold	UPS	210	ASIP/210.	N/A
	Cycling	210	210	FLT test data	Operating
Dynamics	Vibration	810	N/A	FLT test data	; N/A
	Handling	810	N/A	N/A	810

FIGURE 1. Life Cycle Events Versus Environments Matrix

Key for Figure 1

Ref.1 - ETL- 0152, A Digest of High-Temperature
       Storage Literature, U.S. Army Corps of
       Engineers, Engineer Topographic Laboratories,
       Fort Belvoir, Virginia, 22060, July 1978.
UPS - United Parcel Service, Packaging for the Small
       Parcel Environment
210 - MIL-STD-210C Climatic Information to Determine
       Design and Test Requirements for Military
       Systems and Equipment
810 - Environmental Test Methods and Engineering
       Guidelines
ASIP - Air Force Aircraft Structural Integrity
       Program
Repair Tec.- Repair Technology - depends on repair
       processes

DESIGN DUTY CYCLE DETERMINATION

Once the environments for each life cycle event are
identified, the relative duration of exposure to that
environment and operating condition must be determined. The
design duty cycle is determined by answering a series of
questions about situations the product is likely to
encounter at each life cycle event. This process is best
done with a specialist leading a group of people

knowledgeable about the day to day operations of logistics, maintenance and mission use and the engineers responsible for the design.

TRANSPORTATION

Presented are several questions to aid in the development of simulating the transportation environment during the durability test:

1. Is the black box packaged during transportation?

   If it is packaged:

        a. How does that package protect the black box from vibration and shock?

        b. Will the package degrade under effects from moisture, heat or biological attack?

        c. If the black box needs to be protected from moisture by a desiccant and/or protective barrier, for how long is that protection effective? (This topic is further covered in the Storage section)

2. How is the black box transported, for how long and how often?

   a. How is it transported from manufacturing to depot supply, from depot supply to logistics supply and from logistics supply to tactical supply. How often is it transported and how long does it take? **If protective packaging is used, the transportation environment may be insignificant when simulating a lifetime of stresses.**

   b. How is it transported from tactical supply to mission use and how often.? **The black box probably no longer has the protective packaging at this stage and this environment is likely to add to the overall fatigue of materials in the black box.**

   c. How often is it removed from the aircraft and transported to maintenance shops?

1. In peacetime?
2. During combat?

For this case study, the black box is transported in a protective package on a cargo truck (vibration data for cargo trucks are found in MIL-STD-810D for common carriers) from manufacturing to depot supply, from depot supply to logistics supply and from logistics supply to tactical supply. It is usually only transported once to depot supply, but may be transported several times between logistics supply and tactical supply. The protective packaging protects the black box from vibration and shock effects and diurnal cycling is insignificant due to the small amount of time spent during this phase of transportation. For these reasons, this portion of the transportation life cycle event is not considered to effect the overall fatigue of the black box and is not included in the durability test profile for this case study.

However, tactical supply transportation is considered for inclusion in the durability test, because the black box is transported during tactical supply without the benefit of protective packaging (this means that somebody has to take the electronic equipment out of the box before it can be installed on the aircraft). The tactical supply environment may subject the black box to a fairly rigorous vibration and shock environment which may decrease the life of the materials.

Test Parameter Development

For this case study, it is assumed that this black box is removed from the aircraft an average of three times and withstands vibration effects during tactical supply transport for five minutes each time. Therefore, the durability test profile should include a section for simulating the logistics supply transportation environment a maximum of four times for a duration of 5 minutes each time.

STORAGE

The primary parameters to be concerned with storage are location and duration.

1. Where will the black box be stored and for how long?

a. Before shipment?
b. At the Depot Level?
c. At the Squadron?
   1. During peacetime?
   2. During combat?

2. Is this black box packaged for extended storage?

This communications black box will probably not be used upon delivery and may spend up to two years or more in depot storage. For this application, the customer's Systems Requirement Document stipulated that it must operate for 15 years after a two year storage period. (This would be very difficult to contractually enforce because most warranties only last for five years, irregardless of storage time. However, the customer can ask for this requirement as a design parameter) The customer did not specify a storage location.

For purposes of examining the durability of this electronic box, many guidance documents address the meteorological air extremes such as Wet-Warm, Wet-Hot, Hot-Dry, Intermediate cold, Extreme cold, etc. There is not a succinct resource that addresses equipments' response to such meteorological air extremes. Several reports, listed in the references, have attempted to document equipment's response to meteorological conditions under storage conditions, yet the data is not statistically complete.

The guidance documents address how excessive storage temperature and moisture environments will precipitate certain failure modes such as viscosity reduction and evaporation, physical expansion and differential expansion of dissimilar materials, physical breakdown of organic packaging and chemical reactions such as corrosion, electrolysis and oxidation of the electronic materials. (Reference 5). For this application, the majority of extended storage time will be spent in a warehouse in the conditions as listed below, with the electronic black box packaged with a protective moisture barrier and a desiccant. Even though the exterior of the warehouse is exposed to a diurnal cycle, the equipment inside that warehouse is likely to experience a steady state thermal condition due to thermal mass of the stored items. Steady state temperatures do not significantly stress electronic materials. It is the thermal cycling primarily due to power on/off cycling and mission usage cycling which will introduce thermally induced

stresses. However, if it is determined that simulating a
two year storage life to test the durability of the
electronic system is essential, the following conditions
would expose the electronic system to a representative
series of storage conditions.

For this case study, the following environmental
situations were postulated for lifetime storage simulation:

   a. 1 month of dump desert storage conditions
   b. 5 months of storage in a warehouse in an
      intermediate hot climate
   c. 6 months of storage in a warehouse in an
      intermediate cold climate
   d. 12 months of storage in a temperate climate

The approximate steady state condition and duration for
the above conditions are:

   a. 30 days at 43.5°C (Reference 6)
   b. 150 days at 36.5°C (Reference 2)
   c. 183 days at -26.5°C (Reference 2)
   d. 365 days at 14°C (Reference 7)

Test Parameter Development

Temperature and humidity are the primary environmental
stresses imposed upon the electronics during storage.
However, exact duplication of the postulated storage
conditions would not accomplish the test in a timely manner.
Since the primary failure mechanisms in storage are due to
thermal aging and chemical reactions caused from moisture,
the storage portion of the test should introduce the
stresses which would most likely cause the anticipated
failure modes to occur.

High Temperature Thermal Aging - In standard
reliability life testing, it is a common practice to use the
Arrenhius equation for accelerated thermal aging of
electronics subjected to steady state high temperatures.
The Arrenhius equation is a chemist's tool to judge the
reaction kinetics of a single material. The Arrenhius
equation gained wide spread use in the early 50's with the
rocket propulsion type life test then spread to the nuclear
industry for aging of non-metallic material. The Arrenhius

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equation relies extensively on the determination of the
activation energy for the material. To age a single organic
material, using the Arrenhius relationship to accelerate
aging encountered under a steady state thermal load may be
quite applicable. However for aging electronic systems, it
lacks scientific rigor. This quote from Reference 8 clearly
identifies the problems with accelerated aging techniques
for electronics:

> "Accelerated Aging of Assemblies - The
> accelerated aging of assemblies by the
> application of increased stresses (such as
> thermal, chemical, electrical and radiation
> stresses, and increased rate of operation) is
> a simple concept but difficult to put into
> practice on a rigorous, scientific basis.
> Difficulties are encountered with even
> relatively simple systems such as terminal
> blocks. The difficulties which arise with
> electronic instruments practically compel one
> to make approximations and use engineering
> judgement. As a simple example, if
> transistors and capacitors are subjected to
> the same accelerated thermal aging exposure,
> the process will produce a simulated age in
> the transistor of say five years and a
> simulated age of the capacitors on the order
> of hundreds of years. This difficulty is
> multiplied when there are large numbers of
> components with different accelerated aging
> factors. It is further multiplied by the
> absence or uncertainty of the accelerated
> aging factors for many of the components."

One solution is to identify the potential failure modes
due to the anticipated stress situations and to increase the
particular stress level that will accelerate that particular
failure mode. Reference 8 refers to this concept as the
"Weak-Link Analysis."

As mentioned above, applying the Arrenhius equation to
electronic systems lacks scientific rigor, but for our first
order approximation - the method is presented here as a way
to introduce a thermal aging mechanism on non-metallic
material for a "steady state" thermal extreme. Thermal
aging effects will be simulated for conditions a, b and d.
Arrenhius Equation (Reference 9)

$$t_2/t_1 = e^{-((E_a/k_B)(1/T_1 - 1/T_2))} \qquad (1)$$

where:

t_1 = accelerated aging time at temperature T_1
t_2 = normal service time at temperature T_2
E_a = Activation energy (eV)
k_B = Boltzman's Constant ($8.617 \times 10^{-5} eV/^\circ K$)
T_1 = accelerated aging temperature ($^\circ K$)
T_2 = normal service Temperature ($^\circ K$)

Condition A:

$T_2 = 43.5^\circ C = 316.5^\circ K$

$t_2 = 30$ days

$E_a = 1$, a conservative approximation for electronic non
metallic materials

$T_1 = 95^\circ C = 368 \ ^\circ K$

Therefore $t_1 = .177$ days or 4.25 hours

Condition B:

$T_2 = 310.5^\circ K$

$t_2 = 150$ days

$E_a = 1$

$T_1 = 368^\circ K$

Therefore $t_1 = .436$ days or 10.47

Condition D:

$T_2 = 287^\circ K$

$t_2 = 365$ days

$E_a = 1$

$$T_1 = 368°K$$

Therefore t_1 = .05 days or 1.2 hours

To simulate 6 months of hot storage conditions and one year of temperate storage conditions on the non-metallic materials in this communications black box, it should be subjected to approximately 16 hours at 95°C non-operating.

Cold Storage – There have not been methods identified to accelerate the effects of long term exposure to cold temperature storage conditions. Because solder is stronger at cold temperatures and cold storage tends not to "grow" failures, a short time spent in a cold storage soak, may exercise any failure mode likely to be experienced due to exposure to cold storage. For this reason, Condition c would be simulated with a simple cold soak test – 24 hours at -26.5°C.

Moisture – Thermal cycling accomplished during the mission usage simulation portion of this test will introduce moisture to the system and identify the black box's susceptibility to failure from long term exposure to moisture. In situations where dormant storage accounts for a large part of the systems life cycle (i.e. one shot devices such as missiles) aggravated humidity testing may be in order. However, very little work has been done in correlating aggravated humidity testing to the actual time to exposure in the environment.

MISSION USAGE

During mission usage, a variety of both natural and induced environmental stresses are imposed upon the black box. However, for this case study, the effects of low and high cycle fatigue are being determined. The two primary environments being examined during mission usage are thermal cycling which causes low cycle fatigue and vibration which causes high cycle fatigue. Here are several questions to facilitate determining the extent of low and high cycle fatigue during mission usage:

1. In which platform is the black box installed? (For this application – the platform is a fighter aircraft.)

2. How is the platform used, i.e. what are the mission profiles?

3. How is the black box used on the platform, i.e. what are the operating cycles?

4. Where on that platform is the black box installed?

   a. Are there vibration measurements for that location?
   b. What is the mounting configuration?
   c. If vibration or shock dampers are used, how do the damping qualities degrade over time?
   d. If there is cooling air at that location, are there thermal measurements to verify its effectiveness/ necessity?

Mission Profile

     One way to determine the levels and durations of thermal cycles and the duration of vibration exposure is with the mission profile. The aircraft affiliated with this case study had 12 design mission profiles. Reference 10 outlines the method for developing a composite mission profile from a multiple profile aircraft. The composite mission profile generated from the 12 design mission profiles is presented in Figure 2 for Mach number vs. Time and Figure 3 for Altitude vs. Time.
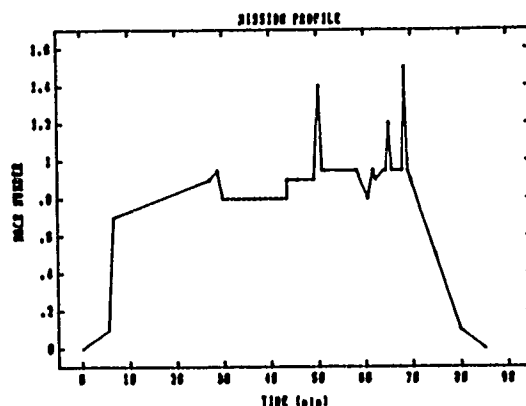
FIGURE 2. Mission Profile Mach Number vs. Time
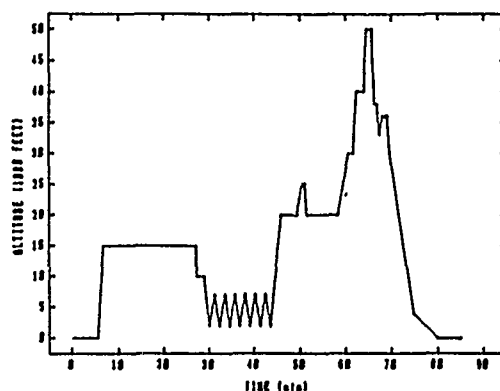
FIGURE 3. Mission Profile Altitude vs. Time

High Cycle Fatigue

High Cycle fatigue is caused by vibration. The largest
cause of vibration on fighter aircraft is aerodynamic
induced turbulence. Aerodynamic induced turbulence is
directly related to the dynamic pressure for the specific
Mach number/altitude combination. Dynamic pressure,
annotated as q, is a function of air density and the square
of the vehicle velocity.

$$q = 1/2 \ d \ x \ v^2 \tag{2}$$

where:

      q = dynamic pressure (N/m^2)
      d = air density (kg/m^3)
      v = Mach number x speed of sound at altitude (m/s)

At low altitudes, the air is densest. Therefore,
aerodynamic induced turbulence is greatest for low level,
high speed flight.

The composite mission profile can be used to develop
the vibration adjustment profile and the equivalent time at
maximum vibration. ** However, the composite mission profile
was developed from design mission usage data, and is good
for highlighting temperature profiles and the extent of
vibration changes for Mach/Altitude combinations. Flight
recorder data obtained after the composite profile was
developed show that more time is spent at low level high

speed flight than originally anticipated. For this reason, the equivalent time at maximum vibration was developed from the flight recorder data, not the composite mission profile.** The adjustment profile is calculated by simply knowing the dynamic pressure for each mach/altitude combination in the composite mission profile. Figure 4 presents the vibration adjustment profile determined directly from the mission profile using the following equations:

Vibration Adjustment:

$$W/W_{max} = (q^2/q_{max}^2) \times k \tag{3}$$

$$dB = 10 \times \log_{10}(W/W_{max}) \tag{4}$$

where:
  W = Power Spectral Density (PSD) (g^2/Hz)
  max = Maximum
  q = dynamic pressure (N/m^2)
  k = Transonic flow factor (Reference 10)
      $k = 1$ for $M < .9$
      $k = .52$ for $M > .9$
  dB = Decibels reduced from maximum
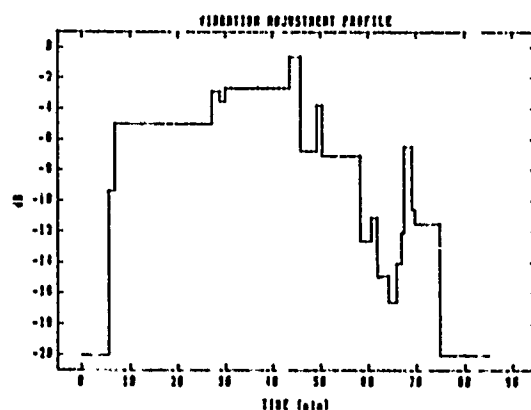
FIGURE 4. Vibration Adjustment Profile

Equivalent Time at Maximum Vibration:

Miner's Rule on Fatigue Damage Accumulation: (Reference 11)

$$D = \sum_{i=1}^{n} n_i/N_i \qquad (5)$$

where:

D = Damage; when D = 1 failure occurs
n_i = number of cycles applied load at stress = 1
N_i = number of cycles to failure at stress from S-N curve

For a linear stress vs. number of cycles (S-N) to failure relationship, the number of cycles to failure will decrease in a proportional amount for an increase in the applied stress. For this application, the aircraft experiences long durations of relatively benign vibration stresses. By increasing the stress level, the same fatigue damage can be accumulated in a shorter time. Figure 5 is an S-N log-log plot for shear fatigue properties of solder from Reference 12.
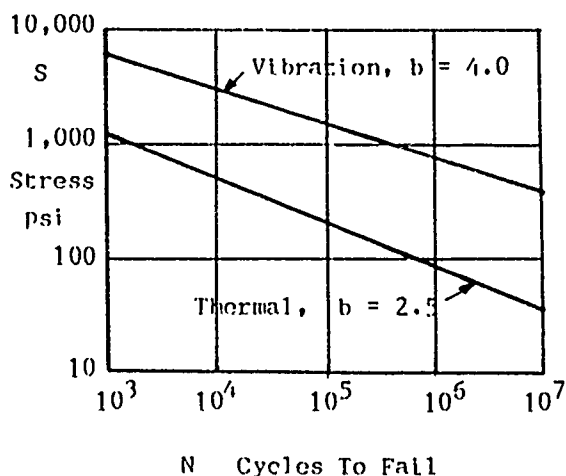
FIGURE 5. Shear Fatigue Properties of Solder

For a sloped line on a log-log plot:

$$N_1 S_1{}^b = N_2 S_2{}^b \qquad (6)$$

where:

N = number of cycles at point 1 or 2
S = stress at point 1 or 2
b = slope of S-N line

For vibration applications, the number of cycles can be represented by time and the stress is in terms of PSD. The application of the fatigue damage accumulation principal to this application leads to the generation of the following equation as highlighted in reference 4:

$$W_0/W_1 = (T_1/T_0)^{1/M} \qquad (7)$$

where:

    W = PSD at condition 0 or 1
    T = Duration of PSD condition 0 or 1
    M = material constant (slope of S-N curve, b)

Reference 4 states that M = 4 for electronic equipment. There is a great deal of discussion on the validity of using 4 as a material constant for all electronic systems and research is being done to obtain values with greater scientific basis. However, for this application, the value of 4 is used to obtain equivalent time at maximum vibration.

By substituting equation 3 into equation 7, the equivalent time at maximum vibration can be determined directly from relative and maximum dynamic pressure and the transonic flow factor.

$$T_{max} = T \times ((q^2/q_{max}^2) \times k)^M \qquad (8)$$

where:

    T_{max} = equivalent time at maximum vibration
    T = time at specific Mach/Altitude block

Test Parameter

Figure 6 presents the flight recorder data for design time vs. actual time and Table 1. shows the values of T_{max} for each Mach/Altitude block for both design time and actual time. Because of Miner's Rule for fatigue damage accumulation, the equivalent time at maximum vibration can be summed to develop the test time to expose the black box to a lifetime of high cycle fatigue at the location specific vibration spectrum. Reference 13 provides a detailed explanation of vibration design and test criteria for avionics systems.
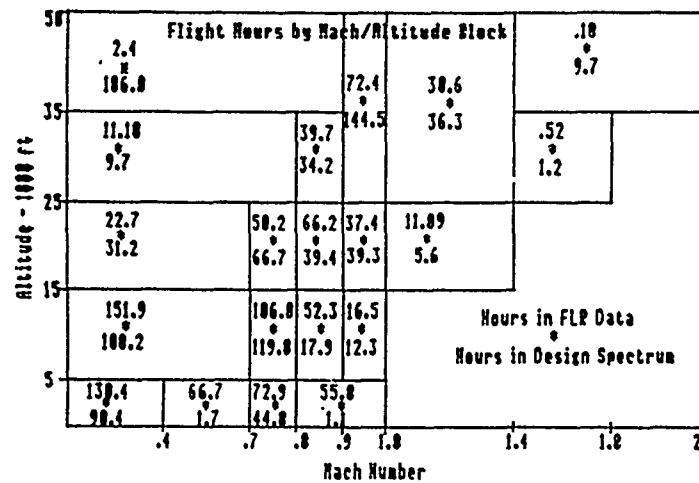
FIGURE 6. Flight Recorder Data

TABLE 1. Equivalent Time at Maximum q for Vibration Test Time (hours)

ALTmin	Mmax	T actual	T max	T design	T max
0	.4	130.39	.0163299	90.4	.0113216
0	.6	66.73	.1010855	1.7	.0025752
0	.7	72.9	1.301298	44.8	.7997005
0	.9	55.8	55.8	1.1	1.1
5	.6	151.94	.0530808	108.2	.0378001
5	.7	106.8	.4387995	119.8	.4922115
5	.9	52.3	11.53573	17.9	3.948174
5	1	16.54	1.502462	12.3	1.117309
15	.6	22.69	.0015120	31.2	.0020791
15	.7	50.2	.0778907	66.7	.1034922
15	.9	66.22	.6771870	39.4	.4029171
15	1	37.4	.3724281	39.3	.3913483
15	1.4	11.09	9.772510	5.6	4.934721
25	.8	11.18	.0006073	9.7	.0005269
25	.9	39.7	.0142489	34.2	.0122749
25	1	72.39	.0102177	144.5	.0203958
25	1.4	30.57	.9409888	36.3	1.117367
25	1.8	.517	.8899494	1.2	2.065647
35	.9	2.396	.0000222	186	.0017251
35	2	.177	.0426723	9.7	2.338536
		997.93	83.54902	1000	18.90012

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Low - Cycle Fatigue

Low cycle fatigue is caused by thermal expansion mismatch of the component lead wire, solder material and multilayer circuit card substrate which causes stresses in the electrical lead wires and solder perpendicular to the plane, of the Printed Circuit Board (PCB). To determine the amount of low cycle fatigue this black box will experience throughout its lifetime, the number and duration of non-operating and operating cycles and the thermal gradient experienced during those cycles must be identified.

Thermal Cycle Determination - Presented here is an Operating Time and Cycles worksheet done with a spreadsheet developed for this particular application:

Operating Time and Cycles Worksheet

The following information is needed before operating time and cycles can be determined.

1. Service Life (years)	20
2. Total Number of Flights	3180
3. Total Flying Hours	6000
4. Utilization Rate (sorties/month)	13.25
5. Break Rate	0.00047

Condition A. Flight operating time and cycles

Assumption: Communications black box on during all flights

A1. Total # operating cycles (2)	3180
A2. Total hours operating (3)	6000

Percent of Total flying hours	100.00%
Percent w/out cooling	100.00%

2. Ground Operating Cycles (On-vehicle)

Condition B. Onboard Power

Ground Checkout - Power up Built in Test for Preflight checkout does not add to the number of operating cycles. However, time while performing pre and post flight checks adds to the total operating time and duration of thermal cycle.

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Power on during Taxi

Taxi time/flight (hours)   0.5

B2. Time on during taxi   1590

DURATION OF THERMAL CYCLES (HOURS)   2.39
(A2 + B2)/A1

Condition C. Ground Power

Mean Time Between Critical Failures

  MTBCF = -Flying hours/sortie   (hours)   4013.51
          /(ln(1-break rate)

Unscheduled Maint.(MTBM)=MTBCF/c.f.
Conversion Factor
 False Alarm rate   0.02
 False removal   0.05
 Tech. Manual error   0.03
      Total   0.1
C.F. = 1 + total   1.1

Mean Time Between Maintenance
MTBM   3648.64

Maint. actions=Flying hours/MTBM   1.64

C1. # cycles = Maint. actions * 2   3.29
    Time/checkout (hours)   0.17
C2. Hours operating during maint.   0.55

Total hours operational w/ground power,   0.55

Ground Operating on-air-vehicle hours
 B2 + C2   1590.55

Percent on Board power   99.97%
Percent External Power   0.03%

Ground operating cycles (on-vehicle)
B1 = 0, see note above   3.29

Condition D. Off Vehicle Operating Cycles

  a) Assumption: There will be no I-level maintenance

b) Assumption: 50% on-vehicle maintenance actions result in sending
   SRU's to depot for repair

ga = # depot maint. actions =   0.82
.5*# On-vehicle maintenance actions
gb = # performance actions/check   2.00
gc = # solder repair/action   1.00
Time/maintenane action (hour)   0.33

D1 = #performance check thermal cycles   1.6
    ga x gb
D2 = Total operational time (hours)   0.54

Condition E. Solder Repair

E1 = Solder Repair Thermal Cycles
        ga*gc   0.82
    Time/solder repair (hour)   0.03

E2 = Total Solder repair time (hour)   0.03

Off-vehicle maintenance hours
D2 = h1 + h2   0.03

Off-vehicle operating cycles
Should split into performance and solder b/c
of major temperature change differences

Total Operating Hours
  A2+B2+C2+D2   7590.58

As this worksheet shows, the thermal cycles generated for
conditions C, D and E (those associated with maintenance
actions) are negligible due to the high reliability of the
communications black box. Therefore, the durability test
can concentrate on simulating the thermal cycles associated
with mission use.

    Thermal Gradient – To identify the thermal gradient
associated with mission use, the temperature rise due to
power on must be identified and the equipment's response to
temperature changes from changes in altitude and Mach number
must also be identified. First, the thermal changes
associated with altitude and Mach Number changes in the
mission profile of the aircraft are identified. Reference 3

provides meteorological data for worldwide air temperature extremes and reference 14 provides data on mean probability of occurrence of aircraft exposure to meteorological extremes for various deployment locations. Next the equipment's thermal profile is identified for the electronic black box operating within the composite mission profile. Equations are presented to calculate aerodynamic induced heating effects. Hot, cold and normal day temperature profiles for ambient thermal conditions, aerodynamic induced heating, equipment bay response and equipment response are presented in figures 7, 8 and 9.

Aerodynamic Induced Heating Equations:

$$T_{ram\ air} = T_{amb}(1+kM^2) \tag{9}$$

$$T_{ad\ wall} = T_{amb}(1+rkM^2) \tag{10}$$

where:
        k = (ratio specific heats-1)/2   k=.2
        r = recovery factor
                r = .85 laminar flow
                r = .9 turbulent flow
        M = Mach Number
        T = Temperature ^{o}K

Reference 15 provides a thorough explanation of Mach Number effects on aerodynamic induced heating. Aerodynamic induced heating profiles are generated assuming turbulent flow along an adiabatic wall.

For this black box, the designer said that the black box would heat up $30^{o}C$ over ambient after 45 minutes Therefore, the thermal time constant is $.67^{o}C/min$, with no external heat sources or sinks. If the external and internal thermal environment were known, a thorough heat transfer analysis would be valuable to determine the extent of thermal cycling that is actually imposed upon the black box. At this stage of the durability test profile development, the heat transfer analysis would be very difficult to perform because there are too many unknowns. The equipment response curves for cold day, hot day and normal day conditions are rough order approximations which use the $.67^{o}C/min$ regardless of the external heat sources/sinks. Data from the aircraft in which this black box is placed, shows that the air in the equipment bay has a

thermal time constant of approximately .91°C/min. The
temperature profile figures 7, 8, and 9 show both bay
temperatures and equipment responses for standard day, cold
day, hot day conditions.

Ambient Thermal Aero. Heating Bay Temperature

Equipment Response

Temperature C
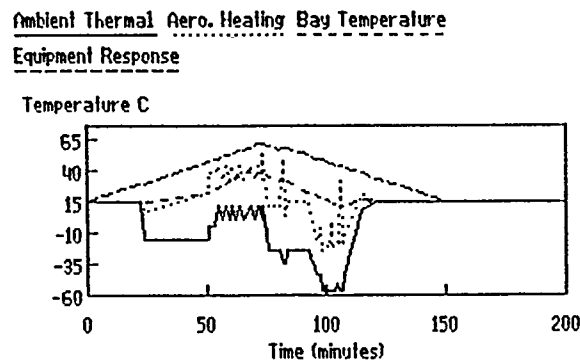
FIGURE 7. Standard Day Thermal Profile

Ambient Thermal Aero. Heating Bay Temperature

Equipment Response

Temperature C
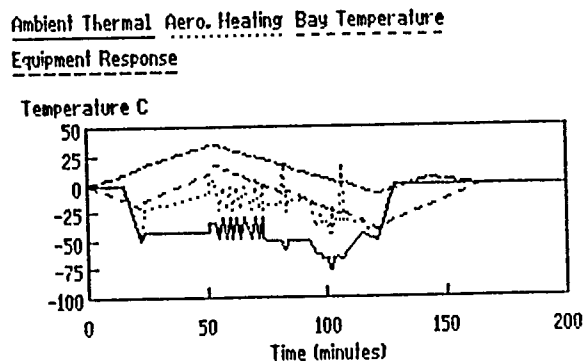
FIGURE 8. Cold Day Thermal Profile

Ambient Thermal Aero. Heating Bay Temperature

Equipment Response

Temperature C
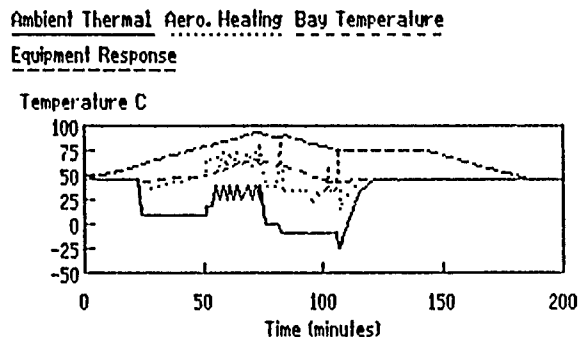
FIGURE 9. Hot Day Thermal Profile

Test Parameters for Low-Cycle Fatigue Excitation

Once an approximation is made on the number, duration
and gradient of thermal cycles, a test can be constructed.
For this example, here are the following assumptions:

1. Standard day conditions
exist 60% of the time
therefore exposing the
electronics to 1908 thermal
cycles with a thermal
gradient of 15°C to 62°C
over a 3 hour and 40 minute
duration, figure 10.
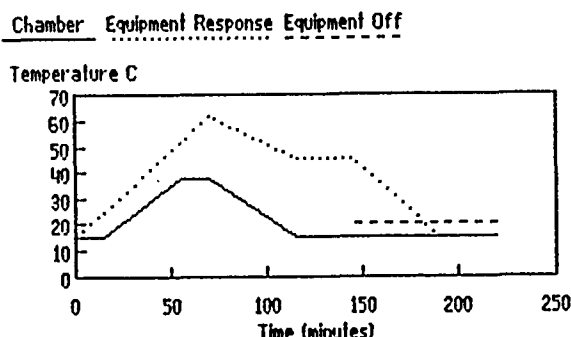
FIGURE 10. Unaccelerated Standard
Day Thermal Test Cycle

2. Cold day conditions
exist 20% of the time
therefore exposing the
electronics to 636 thermal
cycles with a thermal
gradient of -9°C to 36°C
over 3 hour duration,
figure 11.
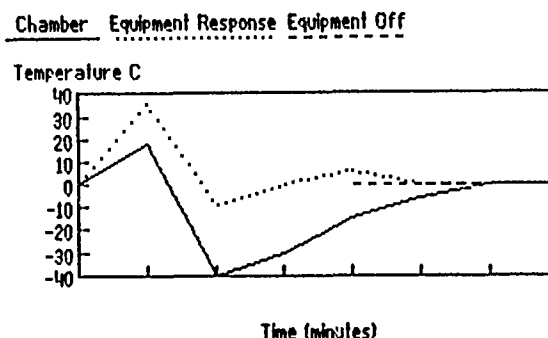
FIGURE 11. Unaccelerated Cold Day
Thermal Test Cycle

3. Hot day conditions exist
20% of the time therefore
exposing the electronics to
636 thermal cycles with a
thermal gradient of 45°C to
94°C over a 3 hour and 40
minute duration, figure 12.
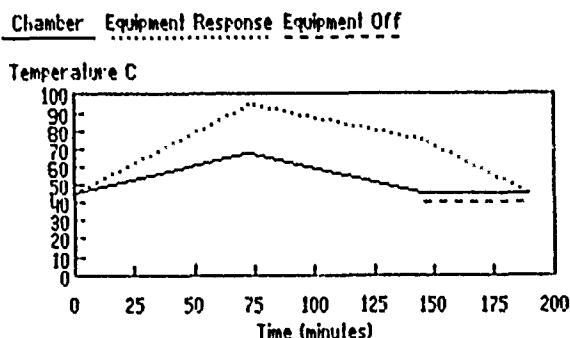
FIGURE 12. Unaccelerated Hot Day
Thermal Test Cycle

4. The primary failure mode will be due to solder fatigue
from thermal expansion mismatch. Workmanship defects will
be eliminated through environmental stress screening
completed as part of the manufacturing process.

5. Stresses introduced due to thermal cycling will cause
linear deformation within the solder. Figure 13 from
reference 16 shows solder response to different temperature
ranges. The linearity assumption has been used with other
analytical techniques for adequate approximations on life
assessment (reference 12). The linearity assumption allows
the test cycle to be accelerated in a simplistic manner.
AT&T Bell Labs has done extensive work on accelerating
thermal cycle test profiles to test the reliability of
surface mounts for commercial applications. However, the
equations are not presented in enough detail within
references 16 and 17 to reproduce the concepts for other
applications. Developing a more rigorous approach for
accelerating non-linear stresses due to low cycle fatigue
for military applications is extremely important for the
successful development of any type of reliability life
demonstration test. Research on this topic must begin
immediately.

RESPONSE OF SOLDER TO STRAINS IN
THE -65°C TO +125°C TEMPERATURE RANGE
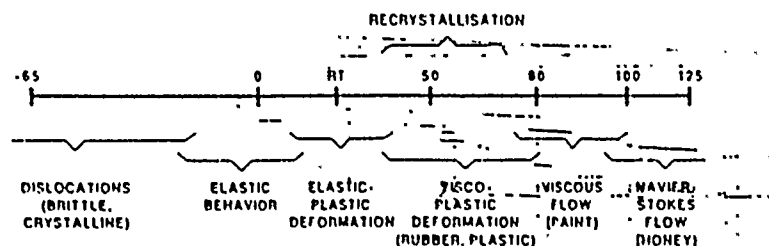
FIGURE 13. Solder Response

Time Compression - It may be desirable to reduce the
test time for simulating low cycle fatigue effects. Methods
to accelerate low-cycle fatigue for military conditions are
not well defined. As mentioned in assumption 5, some work
has been done for accelerating low-cycle fatigue effects on
surface mounts for commercial conditions, but this work is
not presented in a form that is easily applied to other

conditions. For that reason, the following simplistic approach is used to accelerate the thermal cycles affiliated with this case study.

To accelerate the thermal cycles, the following relationships are used:

From Reference 18:

$$N_f = \theta/dy_p{}^B \qquad (11)$$

where:
    N_f = cycles to failure
    θ = ductility for material
    B = fatigue curve slope parameter
    dy_p = applied plastic shear strain

and

$$dy = (L \times da \times dt)/2h \qquad (12)$$

where:
    dy = shear strain
    L = device diagonal dimension
    da = thermal expansion coefficient difference
    dt = temperature change
    h = solder joint height

Even though equation 12 is for elastic shear strain and equation 11 is for plastic shear strain, this statement from reference 18 "Since N_f is proportional to dy raised to the B power, N_f is power-law sensitive to each of the parameters of equation 4" (equation 4 is equation 12 above) gave motivation to substitute the relationship for shear strain from equation 12 for plastic shear strain to obtain the relationship quoted.

$$N_f = \theta/((L \times da)/2h)^B \times dT^B) \qquad (13)$$

and $\theta/(L \times da/2h)^B = C$, constant for the same device

Therefore equation 13 becomes:

$$N_f = C/dT^B \qquad (14)$$

and

$$N_{f1}/N_{f2} = dT_2{}^B/dT_1{}^B \qquad (15)$$

This method increases the temperature change but does not change the cyclic frequency. Reference 18 addresses the importance of maintaining the cyclic frequency when simulating low cycle fatigue effects.

The adequacy of this method for accelerating low cycle fatigue damage by applying a power-law relationship has yet to be verified experimentally. There are a couple of reasons for this:

1. The military has been specifying reliability tests that require thermal cycling from $-55^{\circ}C$ to $100^{\circ}C$. Most of the work to understand fatigue properties of solder does so under extreme thermal cycling conditions; this causes the solder to go from brittle , crystalline dislocations to viscous flow - changes that will never occur in actual use (References 19 and 20) or identifies properties of solder for isothermal conditions under forced mechanical low cycle stress. The industry has been concentrating on designing a product to pass a test - not on identifying the actual operating environment.

2. There are not much data to substantiate the effects of low-cycle fatigue contributions to wear-out. Most electronic failures are due to workmanship defects or design flaws. The maintenance tracking system does not classify failures with the level of detail necessary to determine if the failure was indeed caused by low cycle fatigue. Surface mounted components have brought the topic of low cycle fatigue to the forefront due to their susceptibility to failure from stresses caused by thermal expansion mismatch.

Even though this method has yet to be verified experimentally, the test profile it generates is much more realistic then performing a reliability demonstration test by subjecting the electronics to thermal cycles of $-55^{\circ}C$ to $100^{\circ}C$ at $5^{\circ}C/min$. Temperature cycles such as this are best utilized for precipitating workmanship defects as being defined by ongoing Environmental Stress Screening (ESS) methodologies.

Test Compression using the Power-Law approximations for Low-Cycle Fatigue:

Standard Day

$dT_1 = 47^{\circ}C$

$dT_2 = 72^\circ C$
$N_{f1} = 1908$ cycles
$B = 2.5$ (Reference 12)
$N_{f2} = 656$ cycles
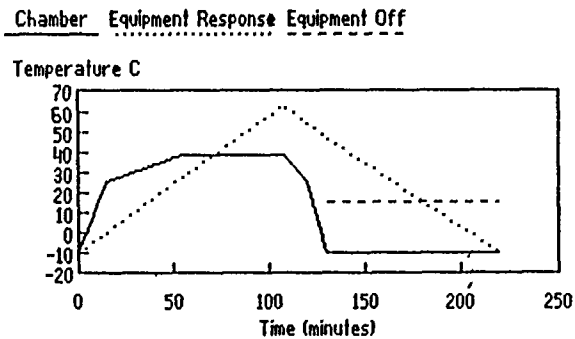
FIGURE 14. Accelerated Standard Day Thermal Cycle

Cold Day

$dT_1 = 45^\circ C$
$dT_2 = 65^\circ C$
$N_{f1} = 636$ cycles
$B = 2.5$
$N_{f2} = 253$ cycles
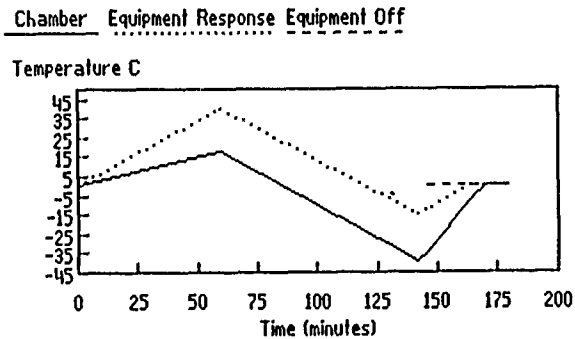
FIGURE 15. Accelerated Cold Day Thermal Cycle

Hot Day

$dT_1 = 49^\circ C$
$dT_2 = 64^\circ C$
$N_{f1} = 636$ cycles
$N_{f2} = 326$ cycles
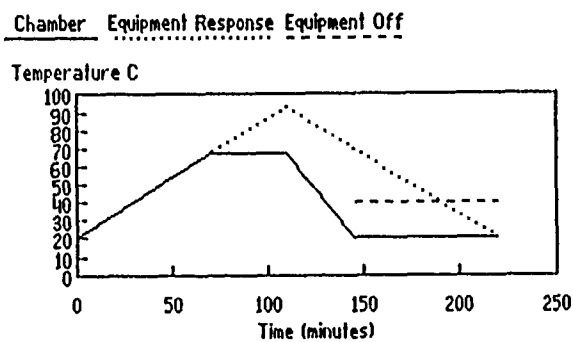
FIGURE 16. Accelerated Hot Day Thermal Cycle

DURABILITY TEST FLOW

Figure 17 is the flow chart for incorporating the different aspects of a durability test for simulating a 20 year service life on this electronics black box. The durability test starts by simulating 2 years of storage life with the black box not operating and under exposure to 95°C for 16 hours. The next step is to simulate transportation as encountered in logistics/tactical supply, without the benefit of the protective package. As mentioned in the transportation section, this is done using a vibration profile found in MIL-STD-810D for a 5 minute duration repeated in the test cycle an additional three times. Low and high cycle fatigue from thermal cycling and vibration encountered during the anticipated service life are simulated starting from point B. For an equivalent of one year of operation this test requires 16 accelerated hot day thermal cycles of 3 hours and 40 minutes each, 33 accelerated standard day thermal cycles of 3 hours and 40 minutes with 4.2 hours of vibration using the location specific vibration spectrum (Reference 13) simulated with the operation of cycles 15 and 16, ending with 13 accelerated cold day thermal cycles of 3 hours. Power on/off is operated as dictated in the accelerated thermal profiles. The test flow shows this one year simulation repeated 19 times to accumulate 20 years of fatigue on the electronic black box.
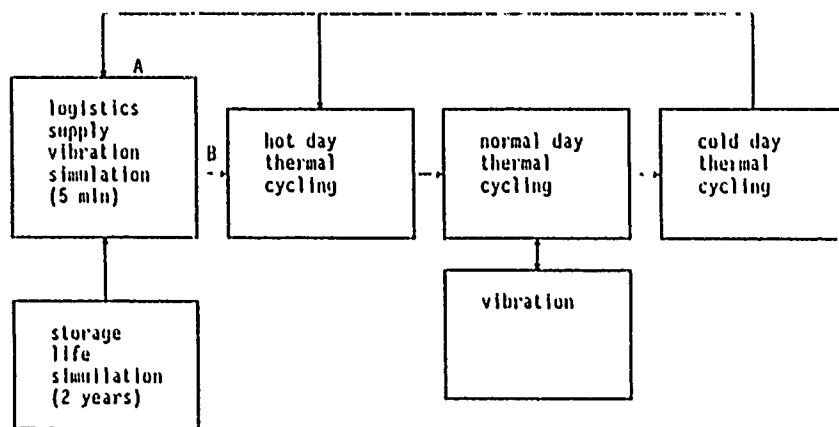
repeat starting at point A 3 times

repeat starting at point B 16 times

FIGURE 17. Durability Test Flow

CONCLUSION

This paper was prepared as a starting point for further research in realistic electronic durability (reliability life) test parameter development. The primary purpose of the paper was to outline a process for realistic test development. This process includes: life cycle environmental characterization, design duty cycle determination, and test profile/parameter development (including time compression methods) for electronic reliability life tests. It is not enough to just identify dynamic and meteorological conditions for differenct life cycle events. To develop realistic life tests (or any other environmental test) it is important to identify the platform and equipment's response to those dynamic and meteorological conditions. Many limitations exist regarding current quality of environmental data, equipment response data and scientific methods for test profile development. By identifying the limitations of the material presented, a base from which to improve is also identified.

REFERENCES

1. ETL - 1052, A Digest of High Temperature Storage Literature, U.S. Army Corps of Engineers, Engineering Topographic Laboratories, Fort Belvoir, Virginia, July 1978.

2. Packaging for the Small Parcel Environment, United Parcel Service Publication.

3. MIL-STD-210C, Climatic Information to Determine Design and Test Requirements for Military Systems and Equipment, January 1987.

4. MIL-STD-810D, Environmental Test Methods and Engineering Guidelines, July 1983.

5. R. M. Seman, et al, Reliability/Maintainability/Testability Design for Dormancy, RADC-TR-88-110, May 1988.

6. H.C. Schafer, Dump Storage Temperatures of Fuel Air Explosive (FAE) Weapons in Shipping Containers - Desert, NWC TP 5138, May 1971.

7. ASHRAE Fundamentals Handbook, 1985.

8. S.P. Carfagno & R.J. Gibson, "Developments in the Qualification of Safety-Related Instruments," ISA Transactions, Vol. 18 No. 2, 1979.

9. J. Foglietta, "Tailoring Thermal Tests Using The Arrenhius Model," 1984 Proceedings Institute of Environmental Sciences Annual Technical Meeting, May 1984.

10. M.L. Lindsley, "How to Develop Life Cycle Environmental Profile Plans," 1987 Proceedings Institute of Environmental Sciences Annual Technical Meeting, May 1987.

11. M.A. Miner, "Cumulative Damage in Fatigue," Journal of Applied Mechanics, Sept. 1945.

12. D.S. Steinberg, "Tools Available for Implementing AVIP," IEEE/AESS Symposium Proceedings, 88TH0238-6, Nov. 1988.

13. M.L. Lindsley, "Vibration Design Criteria for Avionics," Society of Automotive Engineers Aerospace Transactions, 1987.

14. H.C. Schafer, "Quantification of the Thermal Environment for External Carried Aircraft Stores and Ordnance," Journal of Environmental Sciences, Sept. 1981.

15. M.L. Lindsley, Designing for Environmental Stresses, EnRA, Dayton, Ohio, Dec. 1987.

16. W. Engelmaier, "Is Present-Day Accelerated Cycling Adequate for Surface Mount Attachment Reliability Evaluation," NAECON, May 1988.

17. W. Engelmaier, "Surface Mount Solder Joint Reliability: Accelerated Testing & Predictive Modeling," IEEE/AESS Symposium Proceedings, 88TH0238-6, Nov. 1988.

18. R.G. Lambert, "Some Aspects of Solder-Joint Fatigue During Thermal Cycling," 1987 Proceedings Institute of Environmental Sciences Annual Technical Meeting, May 1987.

19. D. Stone, et al, "Mechanisms of Damage Accumulation in Solders During Thermal Fatigue," IEEE Transactions, 1986.

20. H. D. Solomon, "Fatigue of 60/40 Solder," IEEE Transactions, 1986.

21. G.J. Van Wylen, R.E. Sonntag, <u>Fundamentals of Classical Thermodynamics</u>, John Wiley and Sons, New York, 1978.

22. J.P. Holman, <u>Heat Transfer</u>, McGraw-Hill Book Company, New York, 1981.

23. M.L. Lindsley, "AVIP Deciphered for the Environmental Engineering Specialist," <u>1988 Proceedings Institute of Environmental Sciences Annual Technical Meeting</u>, May 1988.

24. MIL-A-87244 (USAF), <u>Military Specification Avionics/Electronics Integrity Program Requirements</u>, July 1`56.

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Research on the Mechanism of Thermal Fatigue in

Near-Eutectic Pb-Sn Solders

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Abstract

This paper discusses the microstructures of solder joints and the mechanisms of thermal fatigue, which is an important source of failure in electronic devices. The solder joints studied were near-eutectic Pb-Sn solder contacts on copper. The microstructure of the joints is described. While the fatigue life of near-eutectic solder joints is strongly dependent on the operating conditions and on the microstructure of the joint, the metallurgical mechanisms of failure are surprisingly constant. When the cyclic load is in shear at temperatures above room temperature the shear strain is inhomogeneous, and induces a rapid coarsening of the eutectic microstructure that concentrates the deformation in well-defined bands parallel to the joint interface. Fatigue cracks propagate along the Sn-Sn grain boundaries and join across the Pb-rich regions to cause ultimate failure. The failure occurs through the bulk solder unless the joint is so thin that the intermetallic layer at the interface is a significant fraction of the joint thickness, in which case failure may be accelerated by cracking through the intermetallic layer. The coarsening and subsequent failure is influenced more strongly by the number of thermal cycles than by the time of exposure to high temperature, at least for hold times up to one hour. Thermal fatigue in tension does not cause well-defined coarsened bands, but often leads to rapid failure through cracking of the brittle intermetallic layer. Implications are drawn for the design of accelerated fatigue tests and the development of new solders with exceptional fatigue resistance.

1.   Introduction

Solder contacts are critical to electronic packaging since they provide both the electrical and the mechanical connection between different levels of the package. As device miniaturization has led to increasingly dense electronic packages the mechanical integrity of the solder contacts has become a serious concern [1-10]. A major problem is thermal fatigue, which arises from the thermal expansion mismatch between the materials joined by the solder. The device is heated and cooled by its own power cycle. Current flow leads

to Joule heating when the device is turned on. The on-off cycle induces a temperature change that may range from room temperature to near 100°C. Specialty devices, such as those used in aerospace avionics, may experience an even larger thermal cycle that results from exposure to the environment, for example, "on" on the ground on a hot summer day to "off" in chill air at 40,000 ft. Military specifications suggest an environmental thermal cycle that varies between extremes at -55°C and 125°C.

The research that is reviewed here concerns the metallurgical mechanisms of the thermal fatigue of near-eutectic Pb-Sn solder contacts on copper, since this is the most common class of contacts in the industry. There are two principal reasons to be concerned about the mechanism of thermal fatigue, and they address the two problems that need to be overcome to ensure joint reliability in service.

First, the industry needs good analytic models or accelerated fatigue tests to guide and verify package designs. While useful tests can be designed empirically, and several have been proposed [10-14], these become uncertain when they are applied to devices, geometries or operating environments outside the set for which they have been specifically verified. A theoretical model or accelerated test is only valid to the extent that it reproduces the mechanisms that lead to failure in service; otherwise it may yield results that are badly misleading.

Second, the industry needs fatigue-resistant solders that can survive the severe conditions that will be experienced in very dense microelectronic packages. The design of improved solders also requires that the metallurgical mechanisms of thermal fatigue be well understood so that appropriate metallurgical modifications can be introduced to defeat them.

From the metallurgical perspective the problem of thermal fatigue in solder contacts is as complex as any fatigue problem that has been researched. Since the solder is mechanically soft and is used at a high homologous temperature (a large fraction of its melting point) deformation is introduced by plasticity and creep (stress relaxation) at both ends of the strain cycle. The cyclic deformation is affected by the fact that the solder contact is a thin layer bonded to relatively rigid materials with a complex intermetallic reaction layer at the bonding line. The long-term deformation behavior is further complicated by the microstructural changes that inevitably occur in the solder as it is cycled and aged. A review of the literature will show that the first-order problem of fatigue crack growth at low temperature under simple periodic loading is only partly understood. There is no reliable predictive theory for thermal fatigue under creep conditions for even simple monolithic materials. The problem of predicting the rate of thermal fatigue in a solder joint is more formidable still, and is unlikely to be solved in the near future. Nonetheless mechanistic research on the fatigue of solder joints can provide valuable information to help guide the development of accelerated tests and the creation of improved solders.

In work published elsewhere we have studied the strength of near-eutectic solders in tension and shear [15], the isothermal and thermal fatigue behavior in tension and shear [16-18], and the creep and stress relaxation of bulk solders and solder joints under shear loads [19,20]. In this paper we concentrate on the mechanisms of thermal fatigue and their association with the microstructure of the solder joint.

2. Experimental Details

To conduct mechanistic research on the fatigue of solder joints one needs metallographic sample preparation techniques to characterize the state of the joint and mechanical testing procedures that can subject solder joints to known loads and loading geometries. Both of these experimental needs present significant problems, and deserve some comment.

The preparation of good metallographic samples from eutectic solder joints is complicated by the fact that the joint consists of a mechanically soft Pb-Sn phase that wets a relatively hard substrate (Cu) through the formation of brittle intermetallic compounds. Metallographic sample preparation is difficult. Some useful techniques are described in reference [15].

The mechanical tests conducted as part of this work include tests to failure in tension and shear to determine the strengths of solder joints in these two configurations, isothermal and thermal fatigue tests under cyclic loading in tension and shear, and isothermal creep and stress relaxation tests under fixed stress (creep) or strain (stress relaxation) in tension or shear.

To accomplish these mechanical tests we require specimens that ensure loading in simple tension or shear under isothermal or thermal cycling conditions. Figures 1-4 show the mechanical test specimens that we have used. The specimen shown in Fig. 1 is designed for isothermal strength and fatigue testing in tension, and has a solder joint in the center of a tension specimen [15,21]. Fig. 2 shows the specimen used for isothermal strength, fatigue, creep, and stress relaxation testing in balanced shear. It consists of a three-layer sandwich of copper plates joined by solder. The sample is notched so that the solder joints in the central region of the plates are in simple shear when the sample is loaded in tension, as can be verified by using scribed specimens [16,17]. Fig. 3 shows the specimen used for thermal fatigue tests in shear [18]. It is a three-layer sandwich of copper-aluminum-copper joined by solder lines. The central aluminum plate is plated with copper, so that the joint is solder-copper on both sides. Thermal fatigue testing is done by alternately immersing the sample in constant temperature baths (usually -55°C and 125°C) for selected periods of time; the strain is imposed by the thermal expansion mismatch between copper and aluminum. Fig. 4 shows the specimen used for thermal fatigue in tension [22]. A specimen that consists of two copper plates joined by solder is inserted

into the aluminum fixture shown in the figure. When the temperature is changed, for example, by immersing the specimen into a heated or cooled bath, the thermal expansion mismatch between the copper and the aluminum imposes a tensile strain across the solder joint. These specimens are useful for fundamental research in that they establish a known macroscopic strain across a solder joint. Other specimen configurations which will not be described here are used to study more realistic joint configurations.
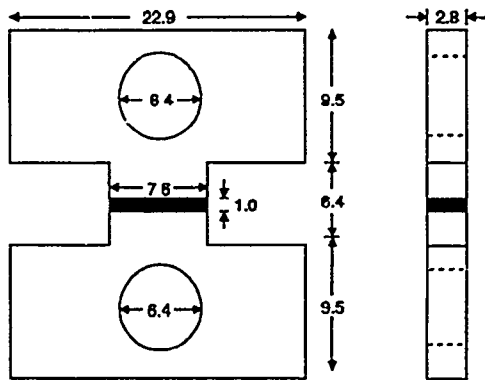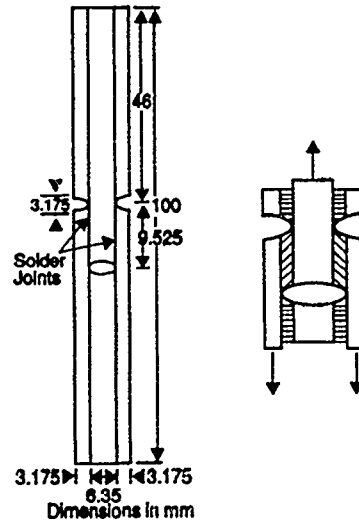
Figure 1.   Figure 2.

Figure 1. Copper/solder composite specimen used for isothermal strength and fatigue testing in tension. The solder joint is the dark shaded region in the center of the specimen. All dimensions are in mm.

Figure 2. Specimen configuration used for isothermal strength, fatigue, creep, and stress relaxation testing. The specimen is a multilayer copper/solder sandwich. On axial loading the two solder joints, shaded regions in figure, are loaded in nearly simple shear. All dimensions are in mm.
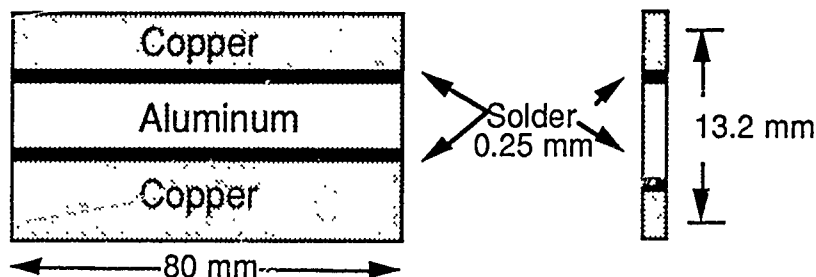
Figure 3. Specimen used for thermal fatigue experiments. The dark central regions are the solder joints. The mismatched thermal expansion characteristics of the constraining copper and aluminium strain the joint in shear with each temperature excursion.
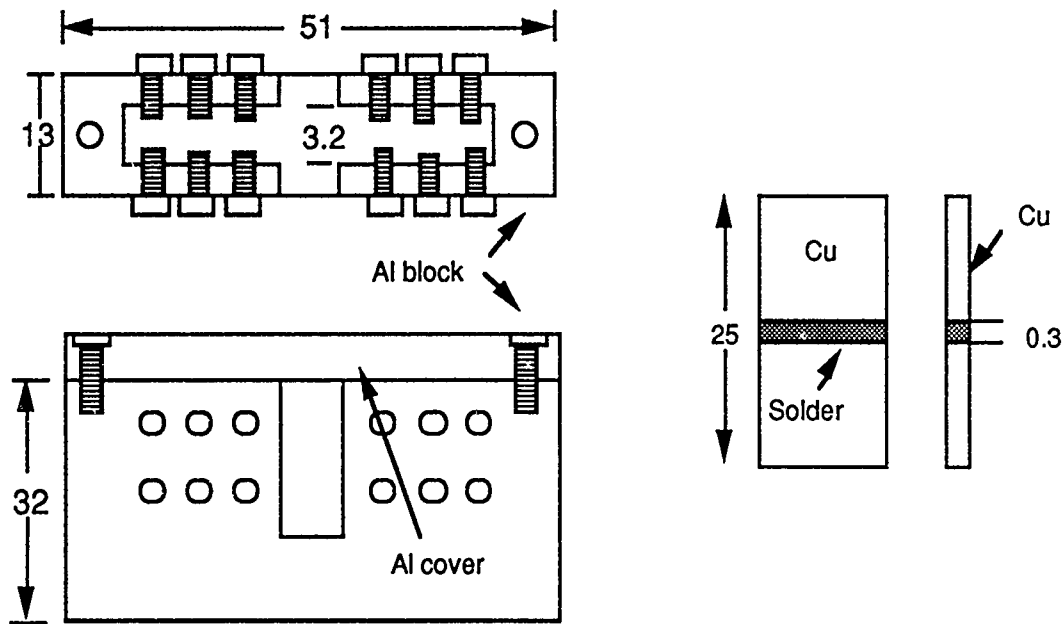
Figure 4. Specimen jig used to perform thermal fatigue in tension. The specimen shown on the right fits into the Al jig on the left. On thermal cycling, the solder joint, shaded region in specimen, is deformed in tension as a result of the uneven thermal expansion between the Al jig and the Cu sample. All dimensions are in mm.

3. The Microstructure of Near-Eutectic Solder Joints

The central principle of Materials Science states that the properties of a material are determined by its composition and its *microstructure*, the manner in which the atoms are arranged on the microscopic scale. It follows that if we are to understand the mechanical behavior of solder joints we must begin with an understanding of the microstructures in which they would most commonly be found. Figure 5 shows a cross-section through a 60Sn-40Pb solder contact on copper at relatively low magnification. The cross-section contains three distinct elements: the copper, the solder, and a thin intermetallic layer along the interface between them. In the cases that interest us here the microstructure of the copper is irrelevant to the behavior of the joint; the stresses imposed are so far below the yield strength of the copper that it behaves essentially as a rigid body. However, both the solder and the intermetallic layer may influence the mechanical behavior of the joint. We therefore describe the microstructures of these.

The interfacial intermetallic layer

The strong adhesion that is established between Pb-Sn solders and copper is due to a chemical reaction between tin and copper that establishes a thin, adherent layer of copper-tin intermetallics along the interface. The intermetallic layer between a near-eutectic solder

and copper is, in fact, a bilayer, as shown in Figure 5. The copper surface is coated by a thin layer of the ε-phase intermetallic, Cu_3Sn, which is separated from the solder by a thicker layer of the η-phase intermetallic, Cu_6Sn_5. The ε-phase consists of small, columnar grains that grow outward from the copper surface. When the ε-phase exists alone, as it does, for example, at the interface of a 95Pb-5Sn solder with copper, the grains are compact and faceted, as shown in Figure 6. The intermetallic is extremely brittle, and fractures easily along the grain boundaries of the Cu_3Sn grains when the surface is bent. The η-phase, on the other hand, presents a very rough interface to the solder. Grains of Cu_6Sn_5 grow out into the solder in spiky, whisker-like crystals of hexagonal morphology, which reflect the hexagonal crystal structure of the η-phase. The morphology of an interface with 60Sn-40Pb is shown in Figure 7. This intermetallic is also brittle. Grains of Cu_6Sn_5 cleave easily under stress.
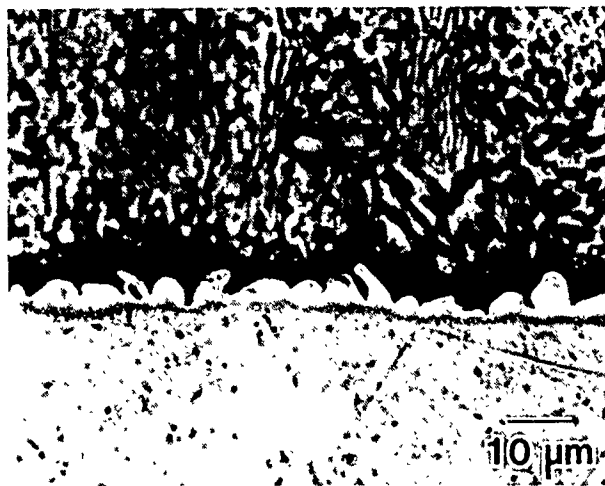
Figure 5. Optical micrograph of a 60Sn-40Pb solder joint on copper. Both intermetallic layers are clearly visible.

Figure 6. Optical micrograph of a 95Pb-5Sn/Cu interface showing the Cu_3Sn intermetallic.
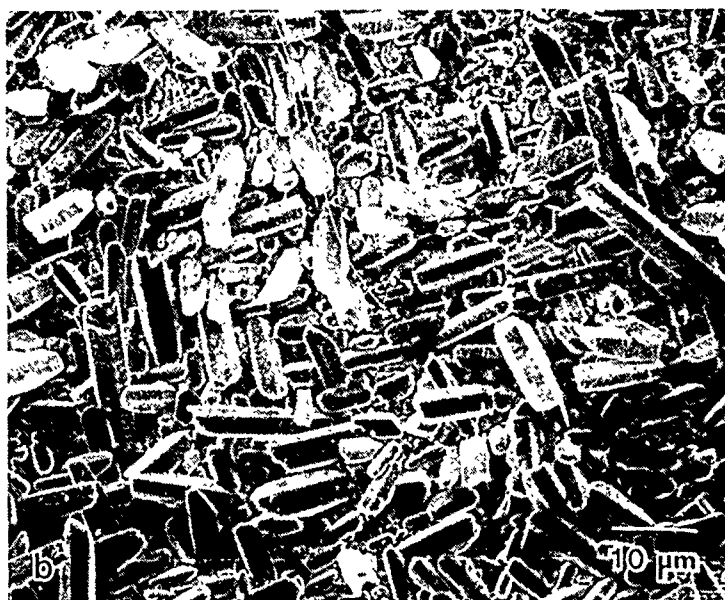
Figure 7. SEM micrograph of a 60Sn-40Pb/Cu interface. The solder has been etched away to reveal the spiky, whisker like crystals of the Cu_6Sn_5 intermetallic.

2 μm
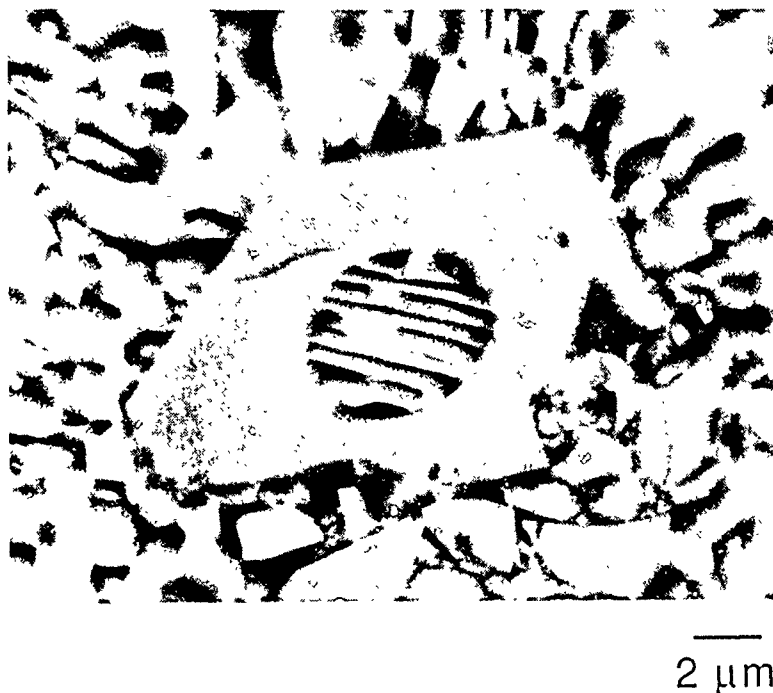
Figure 8. SEM micrograph of a polished 60Sn-40Pb surface etched to reveal the intermetallic morphology. Note that the Cu_6Sn_5 intermetallic takes the shape of a hollow hexagonal rod whose core is filled with solder.

Large η-phase precipitates are also found in the bulk of the solder. These have the curious morphology shown in Figure 8; they are long, hexagonal rods that are hollow along their axes and filled with solder. Specific studies [23] show that these intermetallic precipitates form as whiskers on the Cu surface during initial wetting, break off the surface, and redissolve slightly in the liquid solder before solidification to acquire their hollow appearance. Despite their size, these intermetallic precipitates usually have no more than a secondary influence on the mechanical properties of the solder joint.

Bulk solder

It is important to recognize near-eutectic Pb-Sn solder does not have a unique microstructure, but may be found in any one of several characteristic microstructures depending on the manner in which it was processed. The most common microstructure is shown in Figure 9, and can be understood in terms of the Pb-Sn phase diagram that is shown in Figure 10. A eutectic solder (63Sn-37Pb) solidifies near the eutectic temperature in the phase diagram to form a classic eutectic microstructure that consists of parallel lamellae of Pb-rich phase in a matrix of Sn. The microstructure is divided into grain-like colonies within each of which the Pb-rich lamellae are nearly parallel. These colonies are the features that are referred to as "grains" in much of the technical literature on solder; they are not true grains at all, since they contain two distinct phases and many distinct crystallites.

◄200μm►

Figure 9. Optical micrograph of a typical 60Sn-40Pb solder joint. The dark regions are the Pb-rich phase. Note the phase distribution into grain-like features, i.e. colonies.
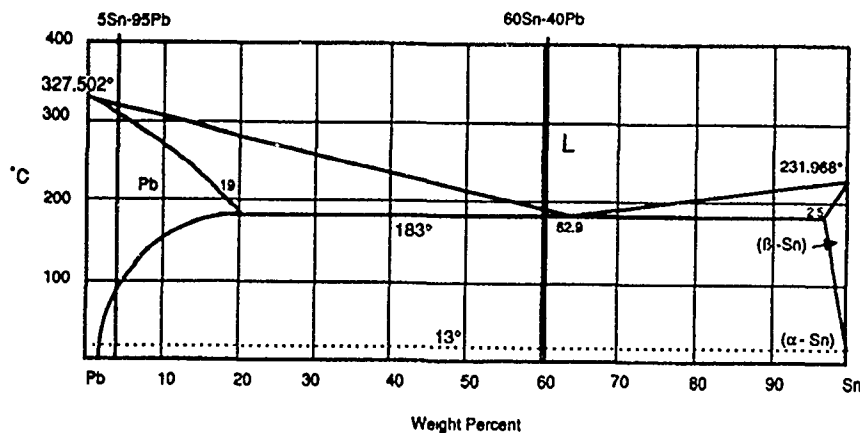
Figure 10. The Pb-Sn phase diagram.

When the solidified solder is cooled to room temperature the solubility of Sn in the Pb-rich phase decreases. The Sn supersaturation is relieved by the formation of Sn precipitates within the Pb-rich lamellae. Transmission electron microscopic studies [27] show that these are plate-like particles of Sn that have stepped surfaces and grow or shrink easily as the temperature is changed to establish an equilibrium Sn concentration within the Pb-rich phase. When the solder is slightly off-eutectic in composition, for example, 60Sn-40Pb, distinct (pro-eutectic) grains of Pb-rich phase also appear.

Figure 11. SEM micrographs of Pb-Sn solder cooled at different cooling rates. The upper most figure underwent the slowest cooling rate, the bottom specimen was quenched. Note the disappearance of lamellar and colony-like features with increasing cooling rate.

As the solder is made to solidify at increasingly high cooling rates the microstructure of the solder changes in that the Pb-rich regions of eutectic become more rod-like and closely spaced and the colony size becomes smaller, as shown in Figure 11. At very high cooling rates the Pb-rich phase may appear in the form of small, equiaxed particles.

The eutectic microstructure of as-solidified solder is unstable because of the very high surface to volume ratio of the grain it contains. If the solder is held at room temperature or above, the eutectic microstructure coarsens through a continuous, diffusion controlled process. The coarsening is particularly pronounced near the colony boundaries, where the grains can reconfigure with relative ease. The coarsening process is slow, but continuous, and has the consequence that the appearance and the mechanical properties, such as strength or hardness, change continuously with time after the solder joint is made.

The coarsening process is strongly accelerated if the solder is deformed mechanically. Mechanical deformation triggers recrystallization at room temperature and above. The microstructure changes into an equiaxed mixture of Sn and Pb-rich grains, as illustrated in Figure 12. Recrystallization is followed by grain growth at a rate that increases with temperature. Recrystallization dramatically changes the mechanical properties of the solder [24]. The recrystallized material is much softer than the same material in the eutectic microstructure, and deforms in creep at a very high relative rate. Recrystallized solder is superplastic, while solder in the eutectic microstructure is not.
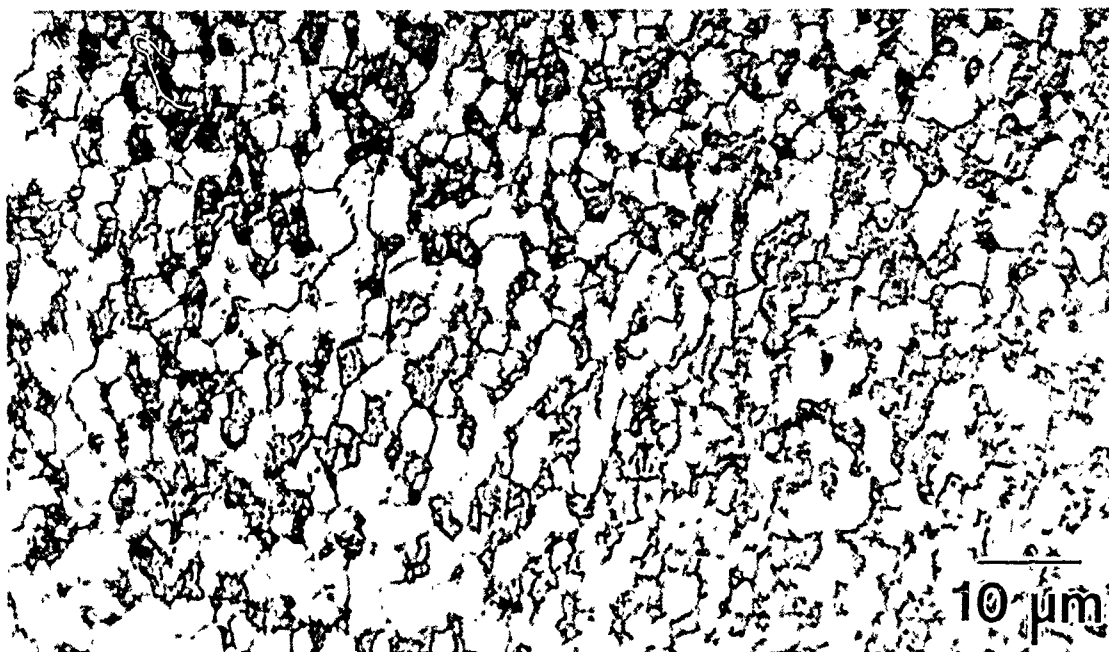
Figure 12. Optical micrograph showing a worked and annealed 60Sn-40Pb microstructure. The thermomechanical treatment results in a recrystallized microstructure consisting only of equiaxed Pb-rich and Sn-rich grains. The recrystallized microstructure bears no resemblance to the initial as-cast one.

Given the variety of microstructures in which near-eutectic solders can be found and the strong influence of the microstructure on mechanical properties, it is hardly surprising that compilations of the quantitative mechanical properties of eutectic solder show a substantial scatter in the measured results.

4. The Mechanism of Thermal Fatigue in Shear

Because the thermal fatigue of a solder joint is driven by the differential thermal expansion of the surfaces that bind the joint, the dominant load on the joint is often a simple shear, and the failure (or, at least, the initial failure) of solder joints in service often occurs in the portion of the joint at which the shear load is applied. For these reasons thermal fatigue under shear loads is of particular interest.

Since there are many possible solder joint configurations and several possible microstructures of the solder in solidified joints, it is quite possibly premature to talk about "the" mechanism of thermal fatigue of eutectic solder in shear. Nonetheless, every test of which we are aware in which a eutectic solder joint was deformed to failure in thermal fatigue, isothermal fatigue, or creep at high temperature under predominantly shear loading led to failure by the same basic mechanism.

The basic mechanism of fatigue in shear

The mechanism is illustrated in Figure 13, which shows the behavior of a 60Sn-40Pb joint as it is cycled from -55°C and 125°C. As the cycling proceeds the shear deformation concentrates into bands that are clearly marked because of the associated rapid coarsening of the microstructure. Figure 14 is a detailed view of a coarsened band. Fatigue cracks grow through these bands, primarily along the Sn-Sn grain boundaries as shown in Figure 14. A review of published cross-sectional micrographs of solder contacts that failed during actual or simulated device operation shows that this fatigue mechanism has been widely observed in near-eutectic solders [9,10], though it is rarely noted.

The mechanism is intimately connected with the evolution of the microstructure and is accelerated by the destructive interference between inhomogeneous shear deformation and microstructure coarsening. Inhomogeneous shear deformation in the solder triggers inhomogeneous coarsening of the eutectic microstructure that is concentrated in the bands of maximum shear. Since the microstructure softens as it coarsens, shear deformation concentrates in the coarsened regions, which therefore coarsen more rapidly. Eventually, cracks form and propagate along the Sn-Sn grain boundaries. Once the Sn grains have failed the Pb-rich phase easily separates to complete fatigue failure.

The microstructural mechanism of thermal fatigue

A closer study of the sequence of microstructural changes that occur during shear failure, whether it is through thermal fatigue [18], isothermal fatigue above room temperature [16,17] or high temperature creep [20,25] reveals the same sequence of internal changes, which can be described as follows.

60Sn-40Pb
Thermal Cycle: -55°C ← → 125°C
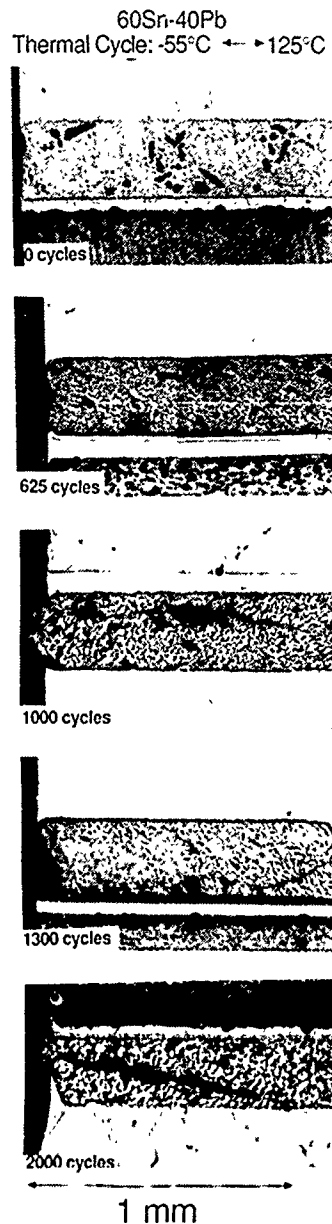
Figure 13. A series of optical micrographs showing the evolution of a coarsened microstructure within the solder joint as a function of thermal cycles.
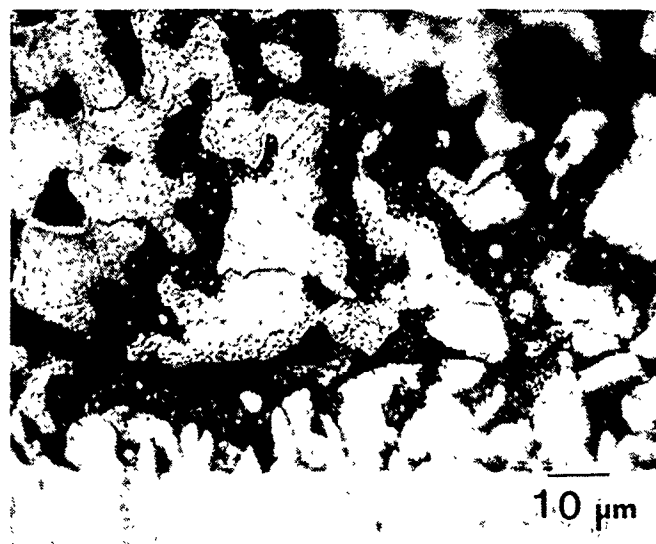
Figure 14. A detailed view of the microstructure within the coarsened band. Note that fatigue cracks grow primarily along the Sn-Sn grain boundaries. (Optical micrograph).

◄002 mm►
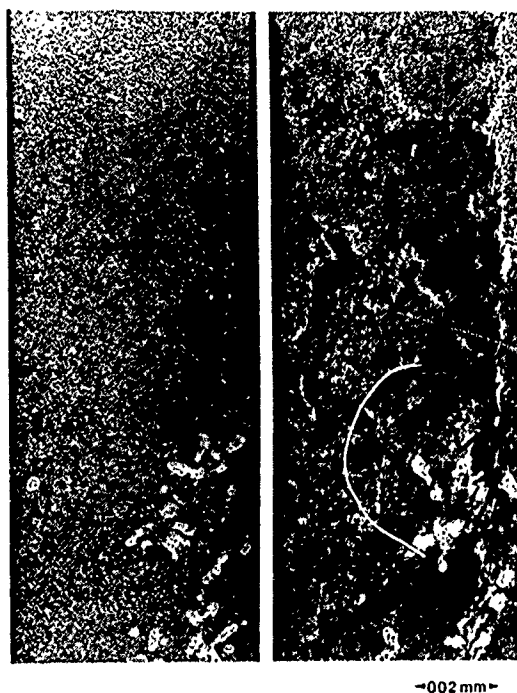
Figure 15. Optical micrograph of a solder joint deformed in creep. On the right is the deformation pattern that develops on the surface of the joint as it is slowly deformed. The micrograph on the left is the same joint after a light polish. Note correspondence between deformation pattern and location of coarsened bands.

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The microstructural event that initiates the pattern of failure is the inhomogeneity of plastic deformation of a eutectic microstructure that is deformed in shear. Figure 15 shows the deformation pattern that forms when a near-eutectic solder is deformed slowly in shear at elevated temperature, as revealed by relief at the surface of the specimen. The deformation pattern includes a nearly straight band of deformation that lies parallel to, but slightly displaced from the solder-copper interface together with several irregular deformation bands that lie approximately perpendicular to the interface and cross the solder joint. A metallographic examination of the same surface after a light polish and etch establishes the correspondence between the deformation bands, Figure 15 right, and the bands of coarsened microstructure, Figure 15 left. Closer inspection shows that the parallel band in Figure 15 crosses eutectic colonies while the perpendicular bands tend to follow colony boundaries. In all cases the parallel deformation band originates at one side of the lateral surface of the solder joint. Finite element analyses [28] suggest that the point of origin is near the principal stress concentration point in the sample.

The mechanism that initiates the coarsened band seems straightforward. It is well known [24] that the eutectic microstructure in the Pb-Sn system is unstable with respect to recrystallization if it is worked at a high homologous temperature or exposed to high temperature after deformation. Inhomogeneous shear strain creates a band of concentrated plastic deformation, which is greatest at the free surface near the stress concentration point. The eutectic recrystallizes there to relieve the accumulated deformation. Since the deformation is local and largely confined to a thin band, only this band of material recrystallizes.

The mechanism of growth of the recrystallized band also seems straightforward. The band grows by the progressive recrystallization of the deformed material. Recrystallization occurs predominantly at the tip of the planar band of previously recrystallized material, and is expected to appear there because this should be the most highly deformed element of material. Since the recrystallized material is soft compared to the eutectic material surrounding it, a narrow band of recrystallized or coarsened material in a eutectic matrix behaves mechanically very much like a narrow crack. Since the applied stress is a simple shear in the plane of the crack the strain field at the crack tip is a mode II deformation zone. The plastic strain field for a mode II crack has been solved for a Von Mises material by McClintock, et al. [26] and is diagrammed in Figure 16. Note that the deformation field is narrow and tends to confine the deformation to the plane of the crack. The next increment of recrystallization near a propagating band of recrystallization that behaves like a mode II crack should occur in the most highly strained material, which lies in the plane of the crack near the crack tip. It follows that the recrystallized band tends to remain plane and narrow while it extends itself along a shear plane, as is observed.

Inhomogeneous shear deformation in the solder triggers inhomogeneous coarsening of the eutectic microstructure that is concentrated in the bands of maximum shear. Since the microstructure softens as it coarsens, shear deformation concentrates in the coarsened regions, which therefore coarsen more rapidly. The preferential coarsening of the Sn

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grains in the shear bands is pronounced (Figure 17). Eventually, the accumulated strain cracks the Sn-Sn grain boundaries. The propagating cracks separate the Pb-rich material to complete fatigue failure.
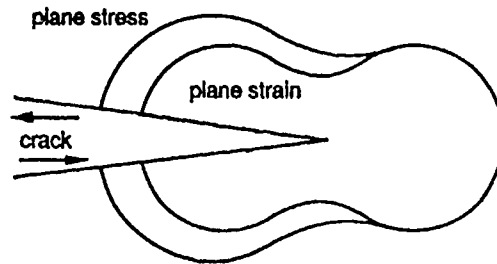
Figure 16. The plastic strain field for a mode II crack.

Features of the shear failure mechanism

There are several features of the microstructural mechanism of shear failure in solder that affect the lifetime of particular solder joints. These include the influence of colony size, joint thickness and cycle frequency on the rate of failure.

It has often been observed that decreasing the apparent grain size of a eutectic solder (which is actually the eutectic colony size) tends to increase its resistance to fatigue [9]. While there is, in fact, very little quantitative data supporting this conclusion, the observation makes sense in terms of the microstructural mechanism of shear failure. A solder with fine colony size deforms more homogeneously in plastic deformation, and is hence more resistant to the formation of the deformation bands that trigger coarsening and failure.

20 μm
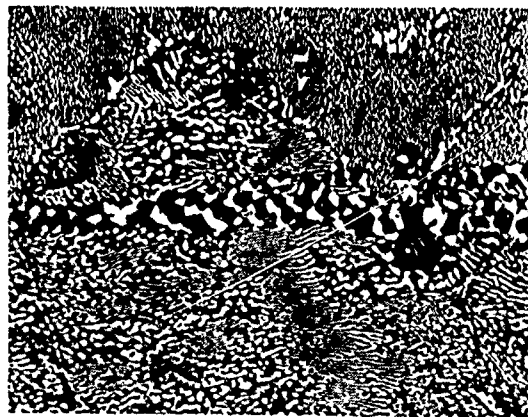
Figure 17. SEM micrograph of a solder joint showing a well developed coarsened band.

Second, arguments based on continuum mechanics suggest that the fatigue resistance of a solder joint should increase dramatically if the joint is made thicker, since this decreases the overall shear deformation per cycle. While there is merit in this approach the thickening of the solder joint is not nearly as effective as one might suppose when the joint is loaded in shear [22]. There are two reasons for this. First, the shear deformation remains inhomogeneous when the joint is made thicker. Once well-developed deformation bands appear, the shear deformation concentrates there, so the local shear in the planar band where failure is actually occurring depends much more on the total strain across the joint than on the joint thickness. The value of a thicker joint is in the smaller initial shear strain, which may retard the formation of bands of concentrated shear. In practice, this beneficial effect is counterbalanced by the slower cooling rate of a thicker joint, which leads to a larger colony size and a greater tendency toward inhomogeneous deformation.

However, there is a significant deterioration in thermal fatigue resistance when the joint is made so thin, or the intermetallic layer is so coarsened by reflow, that the thickness of the brittle intermetallic layer becomes a significant fraction of the thickness of the joint [22]. In this case the crack propagation path may branch out of the ductile solder into the brittle intermetallic layer, causing a relatively rapid failure. An example is shown in Figure 18, which is a micrograph of a cross-section of a 2 mil eutectic solder joint on Cu after thermal fatigue. The crack grows partly through the intermetallic layer.

60Sn - 40Pb
Thermal Cycle: -55°C ↔ 125°C

1500 Cycles

50 μm
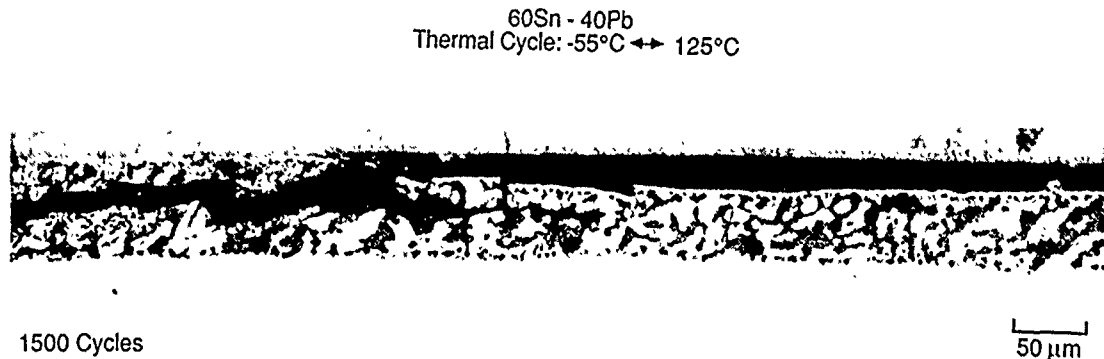
Figure 18. An optical micrograph of a 2 mil eutectic solder joint. Note that the joint failure occurs partly through the intermetallic layer.

Third, since the failure mechanism in shear is associated with recrystallization and grain coarsening, it is driven by shear strain. High temperature contributes to failure because it increases the rate of recrystallization and coarsening, but does not lead to banding or failure by itself. This is illustrated in Figure 20, which shows a cross-section through a solder joint in which the solder continues beyond the end of the joint. Thermal fatigue creates an obvious band of coarsened material in the sheared region within the joint, but results in only a small, overall coarsening in the material outside the joint that has experienced the same thermal cycle without the cyclic shear stress. This has the consequence, which is documented by the thermal fatigue studies discussed in [22] that the joint lifetime in thermal

fatigue is much more sensitive to number of shear cycles than to the total time of exposure at high temperature, and suggests that shear fatigue tests can be accelerated without substantial loss of quantitative information.

60Sn - 40Pb
Thermal Cycle: -55°C ↔ 125°C

1500 Cycles   200 μm
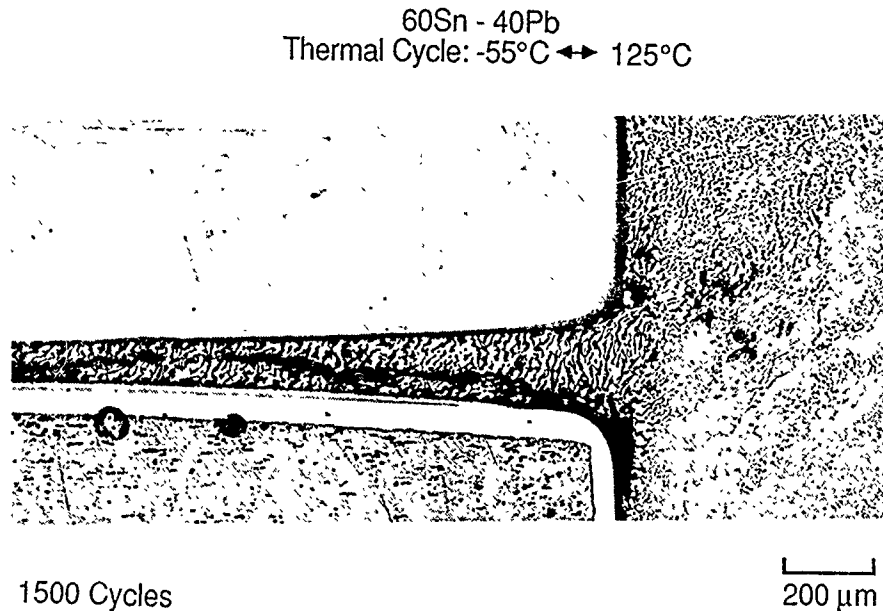
Figure 19. Optical micrograph of a solder joint in which the solder extends beyond the length of the joint. The coarsened band forms only in the sheared solder.

5.   The Mechanism of Thermal Fatigue in Tension

The mechanism of thermal fatigue under cyclic tensile loads perpendicular to the plane of the joint differs significantly from that observed under shear loads [22]. The fatigue failure in tension initiates more rapidly than in shear, and tends to occur through crack growth through the brittle intermetallic layer, as shown in Figure 21. The final fatigue failure contains cracks through the intermetallic that are joined by cracks through the bulk solder near the interface. Bands of coarsened microstructure do not form in the striking way observed for fatigue in shear. The coarsening is more general, and tends to concentrate along colony boundaries perpendicular to the interface, as shown in Figure 22.

The fatigue behavior of solder joints under tensile loads contrasts with that of bulk eutectic solder. The data suggest that solder joints are more liable to failure under tensile load than shear loads, while bulk solder fails more quickly in shear. The reason is the tensile failure of the brittle intermetallic layer. These results suggest that solder joints be designed to minimize tensile loading across the intermetallic. On the other hand, tensile loads are less damaging if they occur in the bulk solder away from the intermetallic, as they do, for example, in the outer regions of the solder attachment of a chip carrier to a circuit board.
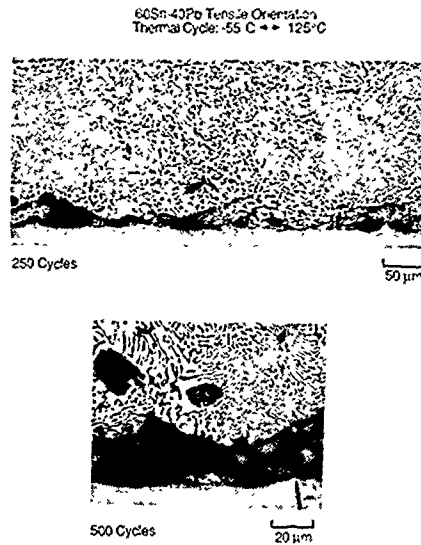
Figure 20. Optical micrograph of a solder joint that has been thermally fatigued in shear. The fatigue failure contains cracks through the brittle intermetallic layer.
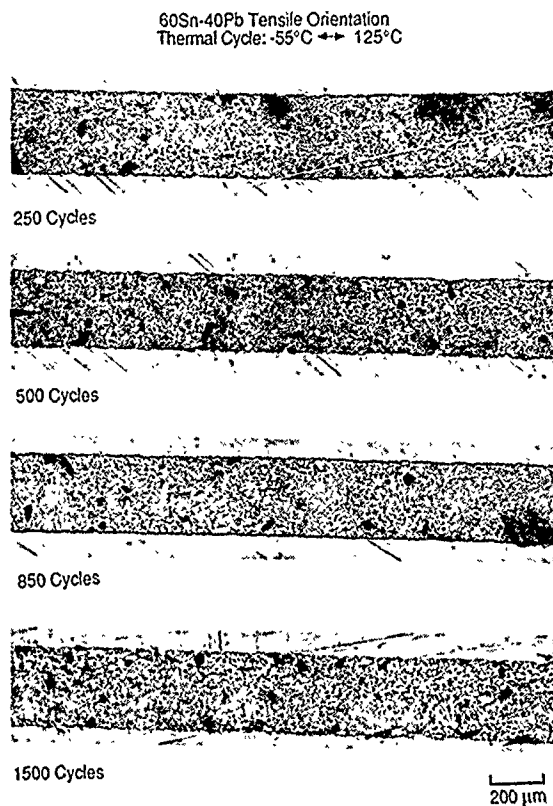
Figure 21. A series of micrographs showing the evolution of solder microstructure as the joint is thermally cycled in tension. The coarsening is general and tends to concentrate at the colony boundaries.

6. Conclusion

The purpose of the work reported here was to clarify the microstructural mechanisms of fatigue in solder to assist in the design of probative accelerated tests and the possible design of fatigue-resistant solders. Its principle conclusions are the following.

While the fatigue life of near-eutectic solder joints is strongly dependent on the operating conditions and on the microstructure of the joint, the metallurgical mechanisms of failure are surprisingly constant. When the cyclic load is in shear at temperatures above room temperature the shear strain is inhomogeneous, and induces a rapid coarsening of the eutectic microstructure that concentrates the deformation in well-defined bands parallel to the joint interface. Fatigue cracks propagate along the Sn-Sn grain boundaries and join across the Pb-rich regions to cause ultimate failure. The failure occurs through the bulk solder unless the joint is so thin that the intermetallic layer at the interface is a significant fraction of the joint thickness, in which case failure may be accelerated by cracking through the intermetallic layer. The coarsening and subsequent failure is influenced more strongly by the number of thermal cycles than by the time of exposure to high temperature, at least for hold times up to one hour. Thermal fatigue in tension does not cause well-defined coarsened bands, but often leads to rapid failure through cracking of the brittle intermetallic layer.

These results suggest that good accelerated tests for the solder joint life in thermal fatigue can be developed, but must be studied with some care to ensure that the mechanism of fatigue is not altered by the acceleration. It appears that thermal fatigue tests can be replaced by isothermal fatigue tests, which are much easier to perform, provided that the isothermal tests study solder joints under controlled load conditions, and are done at sufficiently high temperatures that the microstructural changes that accompany thermal fatigue can occur. Otherwise the test is of limited value. In particular, it would appear that isothermal fatigue tests on bulk solder in tension, which have been proposed as a means for estimating joint fatigue life, are demonstrably useless for that purpose.

The results also suggest that it may be possible to develop solders with fatigue properties that are substantially better than those of the materials now in use. The guidelines for alloy design are relatively clear. The improved solders should deform more homogeneously under shear loads, hence minimizing the strain concentrations that lead to recrystallization and coarsening, and should be compositionally modified to resist recrystallization and coarsening at normal operating temperatures. The challenge is to achieve these material properties.

Acknowledgement

References

1.   E.R. Bangs, R.E. Beal, "Effect of Low Frequency Thermal Cycling on the Crack Susceptibility of Soldered Joints," Welding Res. Supp., 54 (1975), p.377.

2.   J.F. Burgess, R.O. Carlson, H.H. Glascock II, C.A. Neugebauer, H.F. Webster, "Solder Fatigue Problems in Power Packages," IEEE CHMT-7 (1984), p. 405.

3.   E. Levine, J. Ordenez, "Analysis of Thermal Cycle Fatigue Damage in Microsocket Solder Joints," IEEE CHMT-4 (1981), p. 515.

4.   S.K. Kang, N.D. Zommer, D.L. Feucht, R.W. Heckel, "Thermal Fatigue Failure of Solft Soldered Contacts to Si Power Transistors," IEEE PHP-13 (1977), p. 318.

5.   H.N. Keller "Temperature Cycling of HIC Thin-Film Solder Connections," IEEE CHMT-4 (1981), p.132.

6.   E.C. Kubik, T.P.L. Li, "Thermal Shock and Temperature Cycling Effects on Solder Joints of Hermetic Chip Carriers Mounted on Thick Films," Microelectronics Center, Martin Marietta Aerospace, Orlando, FL.

7.   J.T. Lynch, M.R. Ford, A. Boetti, "The Effect of High Dissipation Components on the Solder Joints of Ceramic Chip Carriers Attached to Thick Film Alumina Substrates," IEEE CHMT-6 (1983), p. 237.

8.   J.W. Munfords, "The Influence of Several Design and Material Variable on the Propensity for Solder Joint Cracking," IEEE PHP-11 (1975), p. 296.

9.   R.N. Wild, "Fatigue Properties of Solder Joints," Welding Res. Supp., 51 (1972), p. 521.

10.   E.A. Wright, W.M. Wolverton, "The Effect of the Solder Reflow Method and Joint Design on the Thermal Fatigue Life of Leadless Chip Carrier Solder Joints," Proc. 34th Electron. Compon. Conf., 34 (1984), p. 149.

11. A. Zubelewicz, R. Berriche, L.M. Keer, M.E. Fine; "Lifetime Prediction of Solder Materials," to be published, Journal of Electronic Packaging March 1989.

12. W. Englemaier; "Fatigue Life of Leadless Chip Carrier Solder Joints During Power Cycling," IEEE Trans. Components, Hybrids, and Manufacturing Tech., CHMT-6 (1983), p.232.

13. H.D. Solomon, "Strain Life Behavior in 60/40 Solder," to be published, Journal of Electronic Packaging, March 1989.

14. M.C. Shine, L.R. Fox; "Fatigue of Solder Joints in Surface Mount Devices," *Low Cycle Fatigue* ASTM STP 942, H.D. Solomon, G.R. Halford, L.K.Kaisand, and B.N.Leis Eds. ASTM, Philadelphia, 1987, p. 588.

15. L. Quan, D. Frear, D. Grivas, J.W. Morris, Jr.; Tensile Behavior of Pb-Sn Solder/Cu Joints," J. Electronic Materials, 16 (1987), p. 203.

16. D. Frear, D. Grivas, M. McCormack, D.Tribula, J.W.Morris, Jr.; "Fatigue and Thermal Fatigue of Pb-Sn Solder Joints", Proc. "Effects of Load and Thermal Histories on Mechanical Behavior" Symposium, AIME Spring Conference, Denver, CO, (1987), in Press.

17. D. Frear, D. Grivas, M.McCormack, D.Tribula, J.W. Morris, Jr.; "Fatigue and Thermal Fatigue Testing of Pb-Sn Solder Joints", Proc. 3rd Annual Electronic Packaging and Corrosion in Microelectronics Conf., March 1987, p.269.

18. D. Frear, D. Grivas, J.W. Morris, Jr.; "A Microstructural Study of the Thermal Fatigue Failures of 60Sn-40Pb Solder Joints," J. Electronic Materials, 17 (1988), p.171.

19. D. Tribula, D.Grivas, J.W. Morris Jr., "Stress Relaxation in 60Sn-40Pb Solder Joints," J. Electronic Materials, 17 (1988), p.387.

20. D. Tribula, D. Grivas, D. Frear,J.W. Morris; "Observations on the Mechanisms of Fatigue in Eutectic Pb-Sn Solder Joints", to be published, J. Electronic Packaging, March 1989.

21. D. Grivas, D.Frear, L.Quan, J.W. Morris Jr.;"The formation of Cu_3Sn Intermetallic on the Reaction of Cu with 95Pb-5Sn Solder", J. Electronic Materials, 15 (1986), p.355.

22. D. Frear, D. Grivas, J.W. Morris,Jr. "Parameters Affecting Thermal Fatigue Behavior of 60Sn-40Pb Solder Joints " submitted for publication.

23.   D.Frear, D. Grivas, J.W. Morris, Jr.; "The Effect of Cu_6Sn_3 Whisker Precipitates in Bulk 60Sn-40Pb Solder," J. Elecrtonic Materials, <u>16</u> (1987), p.181.

24.   D.Grivas "Deformation of Superplastic Alloys at Relative Low Strain Rates", Ph.D. thesis University of California, Berkeley, (1978).

25.   D. Tribula, D.Grivas,. D. Frear, J.W. Morris, Jr., in press, Welding Journal.

26.   F.A. McClintock,G.R. Irwin, "PlasticityAspects of Fracture Mechanics", ASTM STP 381 (1965), p.84., as referenced in *Elementary Engineering Mechanics.*, D. Broek, Martinus Nijhoff Publishers 1983, p.99. ;

27.   D. Frear "Microstructural Observations of the Sn-Pb Solder/Cu System and Thermal Fatigue of the Solder Joint," PhD thesis. University of California, Berkeley California, 1987.

28.   F.K. Chen, S. Kobayashi, work in progress.

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DETERMINATION OF THERMAL STRESS RESISTANCE OF
COPPER ELECTROPLATE BY HOT RUPTURE TESTS

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ABSTRACT

Multilayer printed wiring boards make use of electrodeposited copper from two sources. Copper for conductor traces comes from foil manufacturers through thin laminate suppliers. Copper plating for layer interconnection is done in an in-house PTH process. Each source makes use of plating chemicals that are obtained from industry suppliers, but production requirements inherent in foil manufacture or in PTH processing can cause variations that occasionally result in copper deposits that exhibit poor hot strength. In a PWMLB, this can result in corner cracks, barrel cracks and inner layer cracks because some of the copper deposits will be susceptible to fissuring under thermal stress conditions. The phenomenon of hot fissuring is caused by the presence of co-deposited impurities that degrade the hot strength of the deposit due to easy grain boundary separation at elevated temperatures. Stresses imposed by a solder float test, by soldering or by thermal cycling are then sufficient to cause microcracking in a copper plate that is in this condition. In this paper, we describe how changes in the quality of copper plate can be monitored with a hot rupture mechanical test method. By testing plated copper samples before board fabrication, we can detect and evaluate harmful effects such as fissuring before the electroplated copper is used in a PWMLB assembly.

THE EFFECT OF THERMAL STRESS ON COPPER IN A PWMLB

Stresses in the PTH region of a PWMLB are caused by thermal expansion in the thickness (Z) direction when the board is heated. The most likely locations of conductor fracture are shown schematically in Figure 1. These fractures occur in areas of high total strain, i.e., barrel corners, barrel center and the first inner layer. If the thermal cycle that is imposed exceeds the glass transition temperature of the board, still higher strains are possible due to the hydrostatic stresses generated by the movement of the resin in the PWMLB composite.

Fractures in inner layers and in the PTH barrel are intergranular in appearance and similar to those in copper foil where hot fissuring occurs. Cracks in the corners of the PTH barrel are forms of the same failure modes except that the inside corner acts as a stress riser which tends to cause earlier failure. Any of these fractures is likely

PTH BARREL

FOIL INNER LAYERS

Z

MICROCRACKING
REGIONS

REINFORCED POLYMER
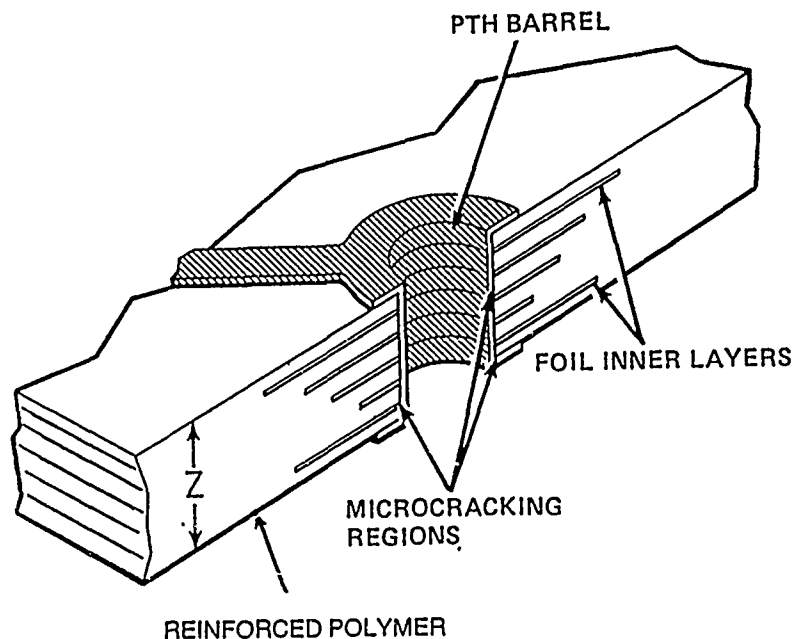
FIGURE 1. Microcracking Regions in a PWMLB

to be expensive because it usually occurs after board assembly or
boardpopulation has been completed. Also, neither of these failure
modes is easily repairable, although PTH fractures are sometimes masked
by filled holes if electrical continuity is maintained by the
conductive filler. On the other hand, inner layer fractures can not be
repaired except by external jumpers, so this failure mode is especially
serious.

AVAILABLE OPTIONS

When PWMLBs are to be subjected to thermal stress, the options
available for avoiding open circuit conditions due to conductor
fracture are: (1) to reduce the Z-direction thermal stress, or (2) to
improve the hot mechanical quality of the copper deposit, or (3) both.

Thermal Stress Reduction

Because of assembly and test requirements, it is not possible to
make PWMLBs without imposing thermal stresses at various steps in the
process. It is, however, possible to reduce the level of this stress.
The most obvious method for doing this is by limiting the thickness of
the board. Z-direction expansion can also be reduced by using a low
expansion resin and constraining reinforcements in the PWMLB laminate.
In addition, a resin with a high glass transition temperature limits Z-
expansion, as well as a hydrostatic effect. Finally, test temperatures
can be reduced to fit application requirements, e.g., instead of

thermal cycling from -65°C to +125°C, do that test from -25°C to +95°C if the application justifies this approach.

Hot Mechanical Quality

Microcracking in electroplated copper is the result of a combination of a thermal stress on an electroplated deposit that is mechanically degraded. Along with more effort to control the bath chemistry, such as is done with the CVS method, it is also necessary to control the hot mechanical quality of the deposit. The hot rupture test that is described in this paper provides a means for monitoring the deposited product from a plating bath and this allows the sorting of plated copper according to thermal stress resistance prior to its use in a PWMLB assembly.

FRACTURE CHARACTERISTICS

Commercial electroplated copper foils can be tested for fracture characteristics by an evaluation of surfaces taken from samples that are fractured at various test temperatures. In this procedure, fracture surfaces are evaluated for evidence of either brittle or ductile fracture. Most plated copper exhibits some degree of ductility at room temperature, therefore, fracture surface analysis is considerably more effective on samples fractured at elevated temperatures.

HOT BRITTLE FRACTURE

In poor quality deposits, plated copper will exhibit either of two fracture modes depending on the temperature at which fracture occurs. At room temperature, a shear component results in tensile elongation prior to fracture. When the same deposit is stressed at 550°F, fissuring at the grain boundaries results in cleavage with very little deformation or elongation prior to its fracture. Figure 2 shows the nature of the fissuring phenomenon where fracture is entirely confined to grain boundaries. The corresponding fracture surface shows the complete absence of shear along with a brittle appearance in the fracture region, and the optical cross-section view shows that no elongation occurred prior to separation.

HOT DUCTILE FRACTURE

Deposits of higher quality exhibit a fracture mode that is the same regardless of the temperature at which fracture occurs. In this material, ductile fractures occur at any stress temperature. Figure 3 shows the fracture conditions in a copper deposit that exhibits hot ductility. The SEM view of the foil shows a ductile fracture with evidence of elongation and no sign of fissuring. The corresponding
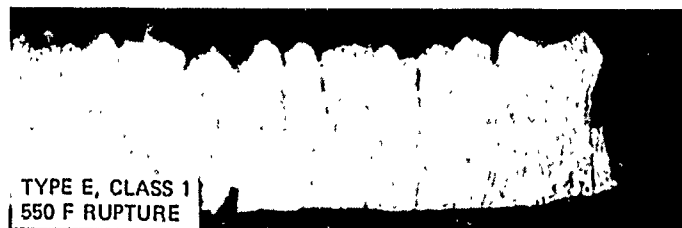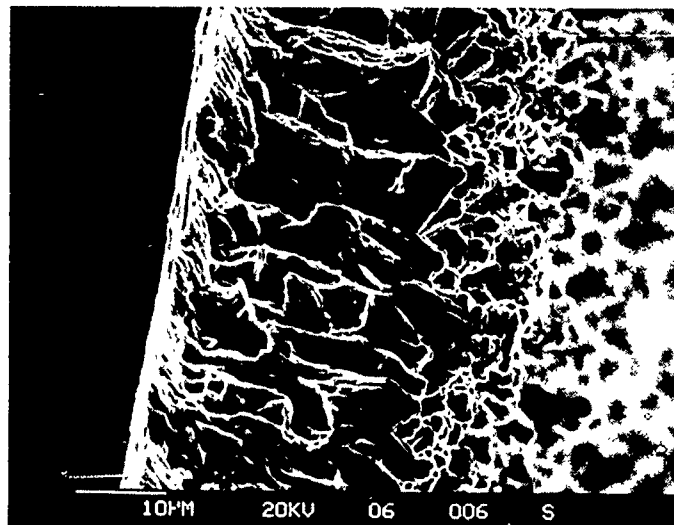
Figure 2.   Hot Brittle Fracture in STD Copper

top   - Fissuring, SEM @ 200X
center - Fracture Surface, SEM @ 1200X
bottom - Fracture, Microsection @ 800X
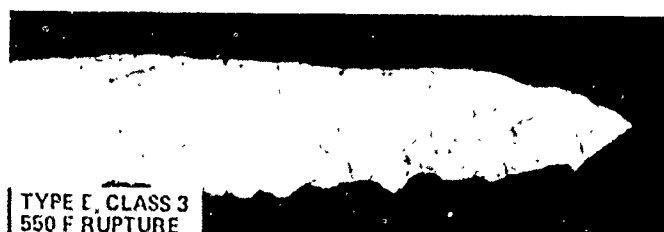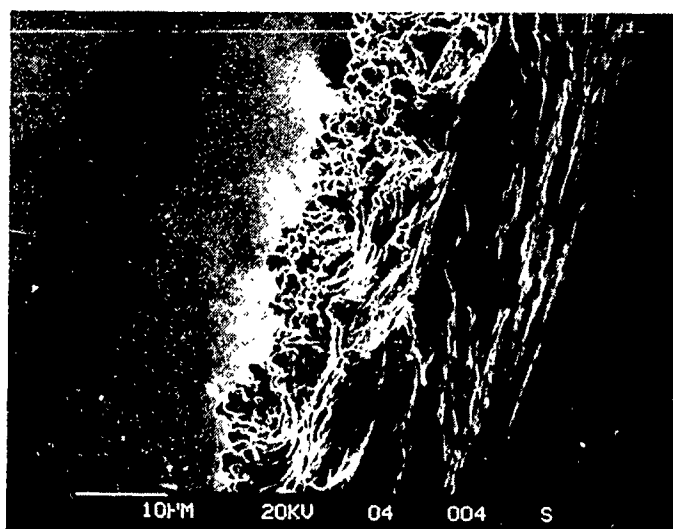
Figure 3.   Hot Ductile Fracture in HTE Copper

top   - Ductile Fracture, SEM @ 200X
center - Fracture Surface, SEM @ 1200X
bottom - Fracture, Microsection @ 800X

fracture surface shows a shear fracture, and the optical cross section view shows considerable elongation in the fracture region.

QUALITY CONTROL

As was shown above, fractography is effective for use in making a distinction between plated copper deposits of two quality levels with respect to hot mechanical characteristics. This procedure , however, is not too well suited for quality control purposes. As was already mentioned, microcracking in copper electroplate is caused by a thermal stress as in a mechanical overload, or by fatigue during thermal cycling. This suggests that a hot mechanical test will be appropriate for obtaining useful information with regard to the microcracking problem. Yet, almost all of the mechanical testing that has been done in the past for control or acceptance purposes has been done at room temperature.

HOT MECHANICAL TESTING

The mechanical properties required of copper foil and PTH copper are specified in IPC-MF-150 and in WS 6536E. The procedures for testing are defined in IPC-TM-650 and ASTM E 345. In the IPC industry standards, there is a requirement for uniaxial tensile testing at 180°C. Otherwise, all of the specified tests are room temperature tests. The uniaxial tensile test procedure at 180°C is cumbersome and time-consuming so its use is not as widespread as is that of the same test at room temperature. Also, there is some evidence that the uniaxial tensile strength values obtained at any test temperature for plated copper are not useful with regard to discriminating and selecting between plated copper samples of different quality levels. Table 1, taken from Reference 1, lists the mechanical properties of two copper foil grades. These results show that the uniaxial tensile values are essentially the same for both grades at both test temperatures. On the other hand, the high temperature tensile elongation values and the hot rupture values show distinctive mechanical differences between these two grades of copper foil. The latter values show that these grades are of widely differing hot mechanical quality.

HOT RUPTURE TESTING

A hot rupture method for testing copper foil has been developed as an alternative to the tensile testing of foil samples. The method provides a convenient procedure for obtaining values for rupture pressure, bulge height, biaxial tensile strength and tangential strain. Furthermore, these values are easily obtained over the temperature range of from room temperature to 550°F (288°C). The proposed test method (IPC-TM-650, Method 2.4.18.2) is presently undergoing evaluation by an industry round robin task group to determine its suitability for

Table 1. Source B: Type E, Grades 1 & 3; - Uniaxial Tensile Reference - 8/18/88)

Foil Type	Lot ID	Test Lab	Test Temp F	Rupture Pressure psig	Bulge Height mils	U.T.S. MD	U.T.S. TD	% Elong MD	% Elong TD
E1	202-144	B	RT	70.4	318	49.7	49.0	11.4	10.4
E1	202-145	B	RT	65.8	316	45.9	45.8	12.8	11.0
E1	202-229	B	RT	59.0	292	44.3	45.2	7.5	9.4
E1	201-168	B	RT	70.9	325	46.2	44.9	11.4	10.4
E1	201-237	B	RT	63.2	279	44.9	45.3	8.5	9.6
E1	201-270	B	RT	60.7	316	43.8	43.2	11.5	10.2
E1	202-144	B	350	32.6	191	24.7	24.2	1.8	1.8
E1	202-145	B	350	35.2	202	22.7	23.3	1.7	1.8
E1	202-229	B	350	29.5	186	23.0	22.6	1.6	1.7
E1	201-168	B	350	31.1	184	23.7	23.0	1.7	1.7
E1	201-237	B	350	30.4	180	21.9	22.3	1.4	1.5
E1	201-270	B	350	30.0	189	22.2	21.7	1.7	1.7
E3	202-40	B	RT	87.9	332	53.1	52.2	18.4	19.2
E3	202-24	B	RT	88.1	355	52.7	52.3	18.6	19.0
E3	9-135	B	RT	80.5	309	51.3	52.0	16.5	19.8
E3	9-147	B	RT	76.7	326	50.6	50.4	17.6	17.5
E3	9-216	B	RT	82.7	275	55.6	55.6	17.9	17.0
E3	202-40	B	350	72.2	333	22.0	22.0	33.4	35.0
E3	202-24	B	350	53.4	242	22.2	21.9	34.8	31.7
E3	9-135	B	350	53.5	259	23.0	23.2	36.6	36.9
E3	9-147	B	350	52.8	267	22.7	22.7	36.9	34.2
E3	9-216	B	350	51.0	207	21.9	21.9	34.1	32.7

MD = Machine direction
TD = Transverse direction

E1 = IPC-MF-150, Type E, Grade 1; STD Copper Foil
E3 = IPC-MF-150, Type E, Grade 3; HTE Copper Foil

use in the specification of the mechanical properties of copper plate for the procurement of copper foil.

The Hot Rupture Test

Rupture testing imposes a biaxial tensile stress on foil test pieces. With the test equipment shown in Figure 4, hot rupture testing can be done as readily as can testing at room temperature. This allows a comparison to be made of mechanical properties as a function of temperature. In this test, the aperture diameter, the test temperature, and the size, density, weight and type of the sample foil are fixed. During testing, an applied pressure causes the sample to bulge in a nearly hemispherical manner. Measurements are made of the pressure and of the bulge height at rupture. From these data, the biaxial tensile strength and the tangential strain can be calculated for foil samples of known thickness, as is explained in Reference 2.

Plated Copper Foil

Typical rupture test samples for commercial copper foil, purchased to existing industry standards, are shown in Figure 5. These 4-inch squares represent the foil lots undergoing the test. Each foil lot is evaluated by testing samples at RT, 350°F and 550°F. For inner layer foils, three pieces tested at each test temperature provide sufficient data for determining average rupture properties.

The corresponding room temperature rupture pressure values are about the same for either Grade of foil. This again indicates that mechanical testing at room temperature will not distinguish between the two grades of foil. However, these results also show that the rupture properties of Grade 1 copper foils decrease drastically as a function of temperature (from an RP of about 80 psig to an RP of less than 23 psig). The rupture properties of Grade 3 foils also decrease with temperature (from an RP of about 80 psig to an RP of greater than 35 psig). However, this reduction is much less than is that for the Grade 1 foil. The difference is wide enough to allow the easy mechanical sorting between the grades through the use of hot rupture tests. As has been mentioned, this difference is due to fissuring in Grade 1 copper.

PTH Copper Deposits

By an extension of the same procedure as described for foils, PTH samples can be tested and evaluated for hot strength. In this process, the test results for PTH deposits are compared with those of standards for Grades 1 and 3 foils, and a judgment is made with respect to the quality of the PTH copper.
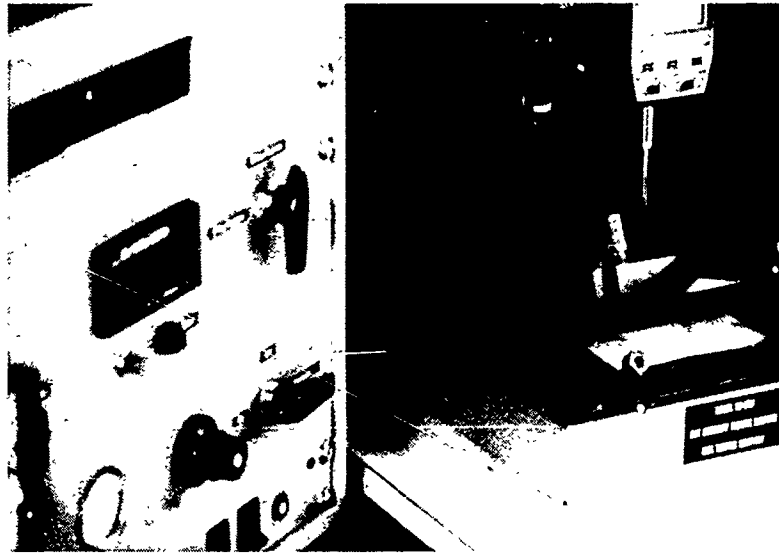
Figure 4.   Hot Ruptured Foil Specimens (2" Aperture)

Top   - EMK Model HD550 Hot Rupture Tester
Bottom, Left   - HTE Copper (550F, 469 mils, 51.4 psig)
Bottom, Right - STD Copper (550F, 280 mils, 20.5 psig)
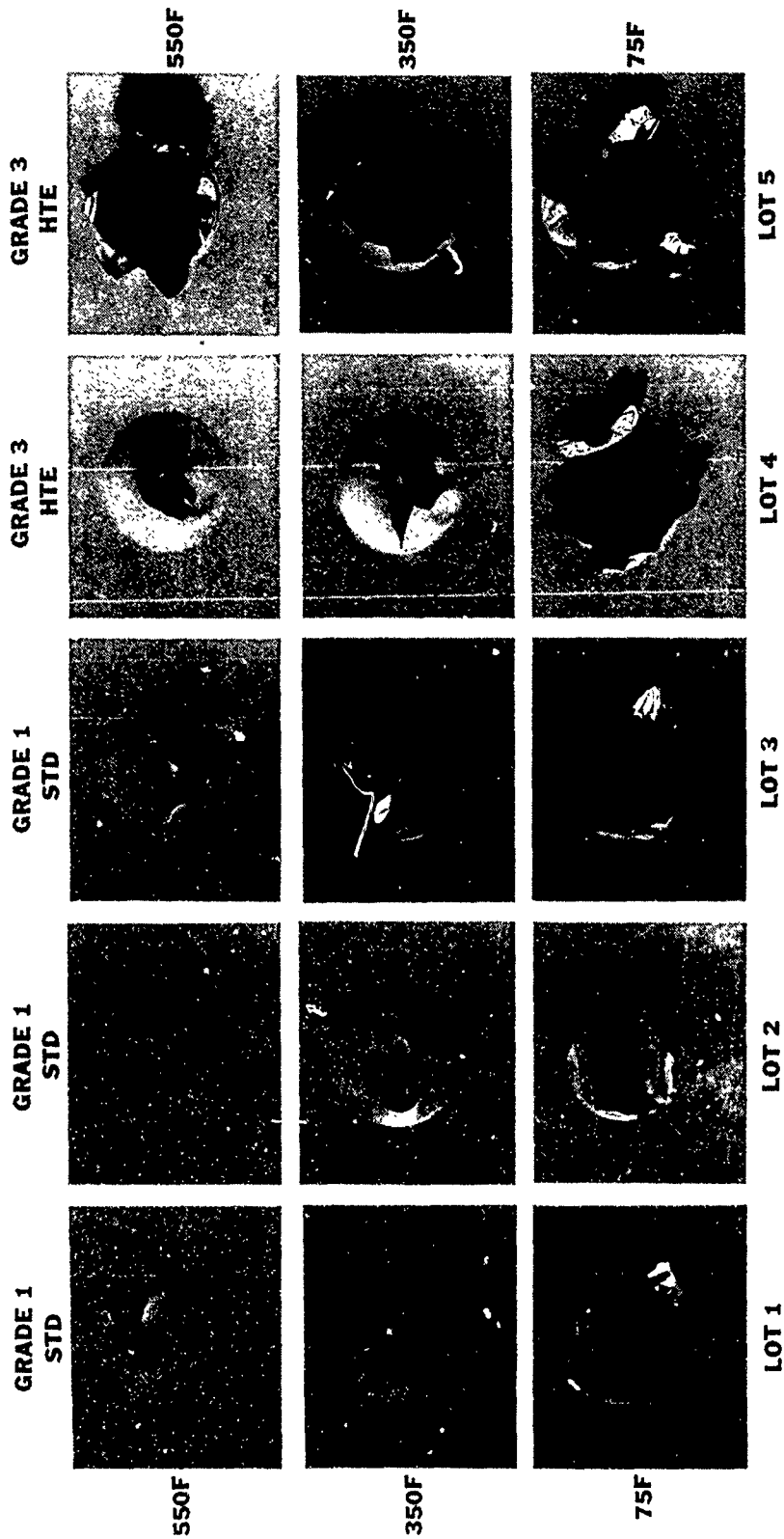
Figure 5.   Hot Rupture Test, IPC-TM-650, Method 2.4.18.2 (Prop)
Commercial Copper Foil, IPC-MF-150, Type E

Figure 6 illustrates the application of this technique. In this figure, the rupture pressure vs temperature plots for Type E, Grade 1 and Type E, Grade 3 commercial copper foils are shown as standard plots. Also shown is a curve made using PTH copper test data. This comparison shows that the copper from the PTH bath has hot mechanical properties that are the equivalent of the Type E, Grade 3 copper foil.

This testing, when extended over a period of time, allows comparisons to be made of the quality of the deposit from a PTH operation with that of standard contols. One such approach is shown in Figure 7 where the objective is to maintain the PTH quality level at that of the Type E, Grade 3 control.

In the case of inner layer foils, mechanical quality that is equivalent to Grade 3 copper has been shown to prevent inner layer cracking in PWMLBs. For PTH copper, only a few controlled studies (see Reference 3) have been made for the purpose of determining the mechanical quality necessary for avoiding barrel cracks, so this correlation has yet to be firmly established.

CONCLUSIONS

I. ELIMINATION OF INNER LAYER CRACKING:

A. This problem is solved by using Type E, Grade 3 foil (not Type E, Grade 1 foil) in thermal stress situations.

B. Hot rupture tests on foils at incoming will provide assurance that foil in use is of Type E, Grade 3 quality.

II. ELIMINATION OF BARREL CRACKING:

A. Type E, Grade 3 equivalent in the PTH seems to prevent fracture.

B. Existing specifications for PTH copper are not adequate for defining Grade 3 quality.

C. Hot rupture and hot tensile elongation are useful for determining Grade 3 quality.

REFERENCES

1. Task Group Report, Metallic Foil Subcommittee, "Copper Foil Rupture Round Robin", IPC, Lincolnwood IL, October 1988.

2. L Zakraysek, "Rupture Testing for the Quality Control of ED Copper", IPC Technical Review, July 1986.

3. R E Belke Jr, et al, "Tailorable CTE PWMLBs for High Density Packages", AFWAL-TR-87-4152, W-P AFB Dayton OH, March 1988.

FIGURE 6. Pressure vs Test Temperature
Acid Copper   PWMLB PTH Production
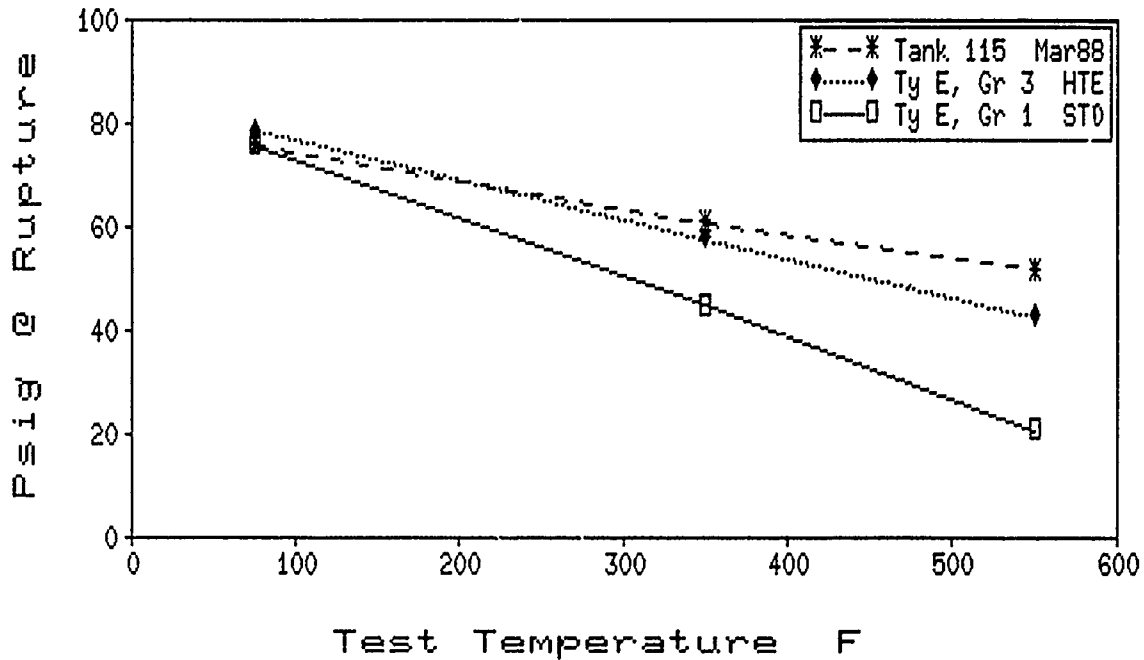
FIGURE 7. PTH Production Quality Control
Acid PTH Copper vs Foil Standards
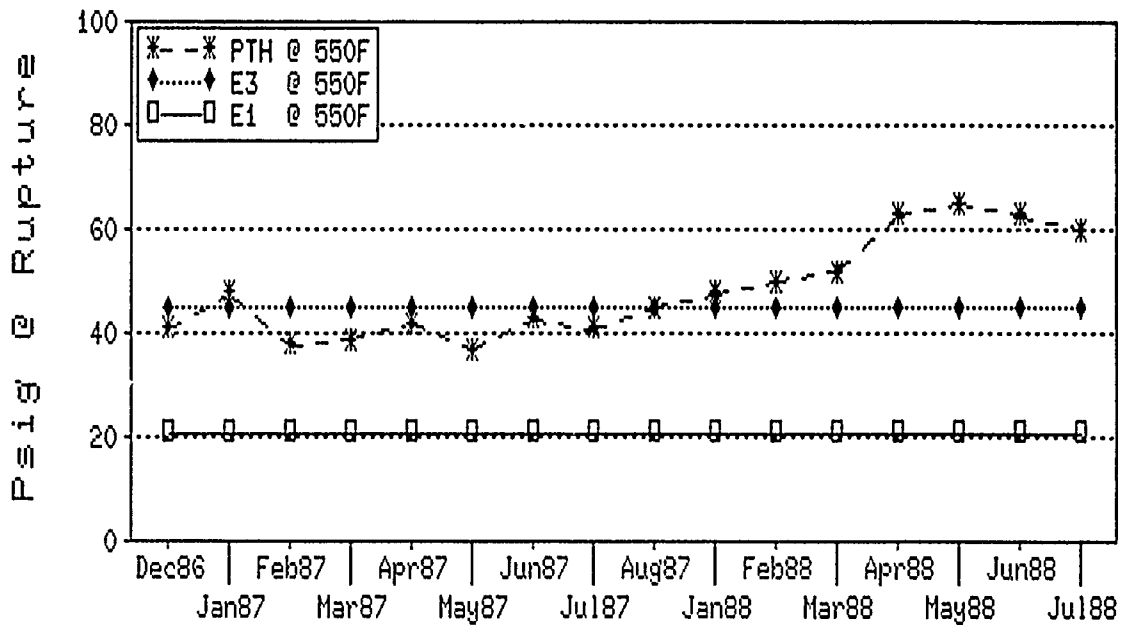
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FATIGUE LIFE PREDICTION FOR LOW-TIN LEAD-BASED SOLDER
AT LOW STRAINS

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ABSTRACT

Fatigue data for low-tin lead-based solder cannot be extrapolated below one percent by Coffin-Manson relation due to non-linearity between fatigue life (log) and strain range(log). The non-linearity is due to the change in this solder's failure mode from mixed transgranular-intergranular (fatigue-creep interaction) fracture at high strains to intergranular (creep) fracture at low strains.

Tensile hold time has a dramatic effect on the fatigue life of solder. A hold time of a few minutes reduces the number of cycles to failure for this solder by an order of magnitude. Further increase in hold time eventually leads to fatigue life saturation. The relation between fatigue life and hold time and the method to calculate the fatigue limit are derived.

A micromechanically-based model for solder has been developed. This model reflects the non-linearity between fatigue life and strain range. In addition, this model can predict the variation of strain magnitude and failure mode with changes in plastic strain range during fatigue.

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INTRODUCTION

Failure of solder joints due to thermal fatigue is a topic of serious and growing concern of the electronics and power industries (References 1,2). Recent advances in electronic design lead to a significant reduction of the strain on the solder joint. However, fatigue life data have not been generated for most solders in this low strain range (less than 1%). Therefore, existing high-strain data are extrapolated to low strains by use of the Coffin-Manson relation (References 3,4):

$$N_f^{\beta} \Delta \epsilon_p = C \tag{1}$$

where $\Delta \epsilon_p$ is the plastic strain range;
β and C are constants.

Since room temperature is approximately one-half of the absolute melting point of solders, a variety of different creep and fatigue processes interact during cycling and can contribute to solder failure at low strain. For example, fatigue crack initiation, fatigue crack propagation, void (creep) initiation, void (creep) propagation, or a combination of these phenomena can be present and lead to non-linearity between fatigue life and strain range. Hence, the Coffin-Manson relation may result in misleading fatigue life extrapolations.

While the frequency effect on the fatigue of lead and solders was studied extensively (References 5,6), the effect of hold times was not investigated in detail prior to our research (References 6-8).

In this paper the effects of strain range, temperature and tensile hold time on solder fatigue at low strain ranges are demonstrated. An analytical micromechanically-based modeling of this solder is offered along with the experimental investigation.

EXPERIMENTAL PROCEDURE

The research was done with low-tin lead-based solder containing 3.5wt.% Sn and less than 0.1wt.% impurities.

Bulk specimens were cast in a flat open aluminum mold (preheated to 175-185°C). Solder was overheated to 375-400°C. After casting, the specimens were machined flat and then homogenized at 175°C for 100 hours. A second anneal at 150°C for 2 hours was done approximately one week before testing to standardize testing conditions since age hardening was detected. Coarse grains (from 50 micrometers to up to one millimeter) produced by casting were divided into subgrains 25 to

100 micrometers long.

All mechanical testing was done in strain control on an MTS servo-valve controlled electrohydraulic testing machine. Fatigue test were done in pull-pull, i.e., the strain varied during testing from zero to the maximum value (0.3 to 0.75%). While the total strain varied from zero to maximum strain during cycling, the values for peak tensile and compressive stresses were almost equal due to high plastic strain in solder. Two types of tests were performed: continuous saw tooth wave tests and tests with hold time at maximum strain (tensile hold time).

Heating and cooling of the specimens were done through the grips of the testing machine by the aid of an apparatus developed at Northwestern University (Reference 9). Specimens were kept in the grips of the testing machine for 2 hours at the testing temperature before the start of cycling. Testing was done in air of approximately 50% relative humidity.

Testing in the strain control mode causes cycling hardening of the solder under investigation. This continues until a saturation stress value is reached. Then due to microcrack growth there is a decrease in the value of maximum stress. The cycle number corresponding to the maximum value of tensile stress was defined as the number of cycles to failure in this research.

RESULTS AND DISCUSSION

EFFECT OF STRAIN RANGE AND TEMPERATURE ON FATIGUE LIFE

Figure 1 shows the dependence of the fatigue life of this solder on plastic strain range at temperatures from 5 to 100°C. It is evident that the data for each temperature (except for 5°C) cannot easily be fit to a single log-log straight line. The data are much better represented by two straight lines with a breakpoint at approximately 0.3% plastic strain. Actually, behavior is even more complicated as discussed later. Thus, the Coffin-Manson relation cannot be used for extrapolation of experimental fatigue data for this solder from high to low strains. However this relation may be used for data extrapolation in two narrow strain range regions (above and below 0.3% plastic strain) with different values of constants in the Coffin-Manson equation.

We attributed the non-linearity in fatigue life (log) - plastic strain range (log) relation to the changes in this solder's failure modes from mixed transgranular-intergranular (fatigue-creep

interaction) fracture at high strains to intergranular (creep) fracture at low strains (Figures 2,3).
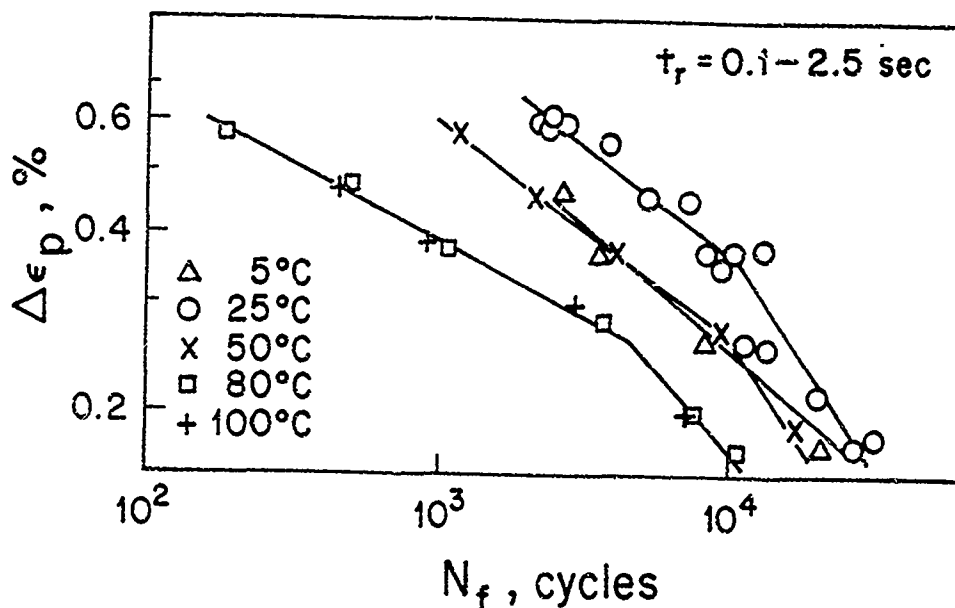
FIGURE 1. Number of Cycles to Failure vs Plastic Strain Range. No Hold Time.

The fatigue life of this solder at 80°C is essentially the same as at 100°C (Figure 1). The change in fatigue life with increasing temperature may be associated in part with complete dissolution of tin precipitates in the matrix above approximately 80°C. No microstructural changes where observed when the testing temperature was reduced from 25 to 5°C. Therefore decrease of fatigue life of solder at 5°C should be studied further. In part, the reduction in fatigue life may possibly be due to a reduction in ductility on cooling.

Thus, extrapolation of results of isothermal tests for 96.5Pb-3.5Sn solder is possible only in the 25 to 80°C temperature range. And even in this narrow temperature range activation energy of solder fatigue is a function of strain range varying from 25 KJ/mole at low strain to 45 KJ/mole at high strain.

Our work shows that the Coffin-Manson relation is not the best choice in isothermal fatigue life prediction of 96.5Pb-3.5Sn solder.

However, limited extrapolation of fatigue data within the 25-80°C temperature range is possible with use of the following constants in the Coffin-Manson relation (Reference 6):

$$\beta = 0.69 - 0.0027\ t^0 \quad (< 0.3\%\ \text{plastic strain}) \quad (2)$$
$$\beta = 0.48 - 0.0028\ t^0 \quad (> 0.3\%\ \text{plastic strain}) \quad (3)$$
$$C = 1.41 - 0.0169\ t^0 \quad (< 0.3\%\ \text{plastic strain}) \quad (4)$$
$$C = 0.19 - 0.0022\ t^0 \quad (> 0.3\%\ \text{plastic strain}) \quad (5)$$

where t^0 is temperature in degree C.

FIGURE 2. Scanning Electron Micrograph of Surface of Failed Specimen. Total Strain Range 0.75%. 25°C. Ramp Time 2.5 sec. No hold.

EFFECT OF TENSILE HOLD TIME ON FATIGUE LIFE

Tensile hold time, i.e. hold time at maximum strain, has a
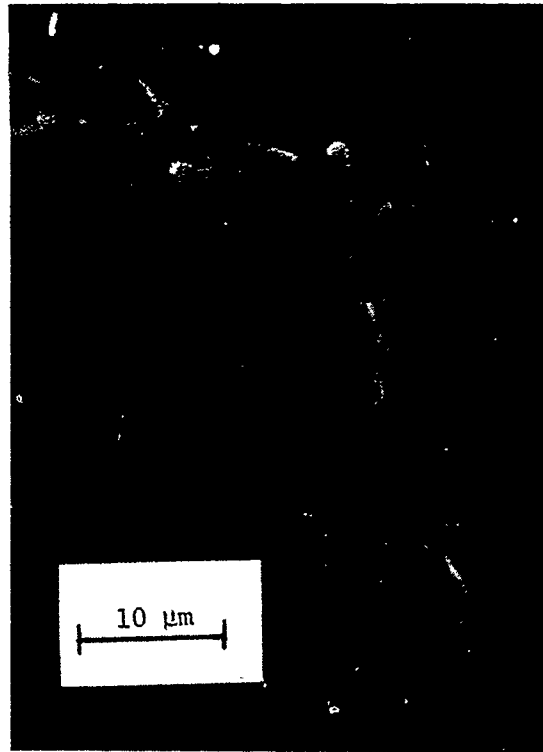
FIGURE 3. Scanning Electron Micrograph of
Surface of Failed Specimen. Total Strain
Range 0.30%. 25°C. Ramp Time 2.5 sec. No hold.

dramatic effect on the fatigue life of many alloys including solders.
A hold time of a few minutes reduces the number of cycles to failure
for solder under investigation by an order of magnitude. Further
increase in hold time eventually leads to fatigue life saturation
(Figure 4). To find a mathematical relation between the number of
cycles to failure and tensile hold time the time to failure is plotted
versus tensile hold time in the Figure 4. As previously discussed
(References 6,8) the following linear relation between fatigue life
and tensile hold time per cycle exists:

$$t_f = A + B\ t_{th} \tag{6}$$

where t_f - time to failure;
      t_{th} - hold time at maximum strain (tensile hold).

Since time per cycle, t_c, is equal to :

$$t_c = 2 t_r + t_{th} \qquad (7)$$

where t_r - ramp time,

the number of cycles to failure can be found as:

$$N_f = \frac{t_f}{2 t_r + t_{th}} = \frac{A + B t_{th}}{2 t_r + B t_{th}} \qquad (8)$$

Since in the present study the ramp time is much less than hold time, ramp time can be neglected and finally:

$$N_f = \frac{A}{t_{th}} + B \qquad (9)$$

For the case of long hold times, the first term in Equation 9 becomes negligible and

$$N_f = B \qquad (10)$$

From Equation 10, the limit in the number of cycles to failure under a given set of conditions is equal to the slope of a line in time to failure-tensile hold time per cycle coordinates (Figure 4). Thus, solders will survive not less than B number of cycles with any tensile hold time in the cycle under given strain range, ramp time and temperature. Equations (9) and (10) were found to hold for other solders and other materials also (Reference 10).

Figure 5 shows the relation between the number of cycles to failure and the plastic strain range in tests with and without tensile hold time. The no hold curve is a redrawing of the curve in Figure 1 with a much better fit to the data. It is obvious that the Coffin-Manson relation does not hold.

Using Equation 9, the data for several strain ranges were extrapolated to higher tensile hold times, and approximately the same numbers of cycles to failure were found, as shown in Figure 6. These are essentially plots of N_f' values. Thus, it is necessary to perform just a few tests with hold time in the cycle at each strain range to

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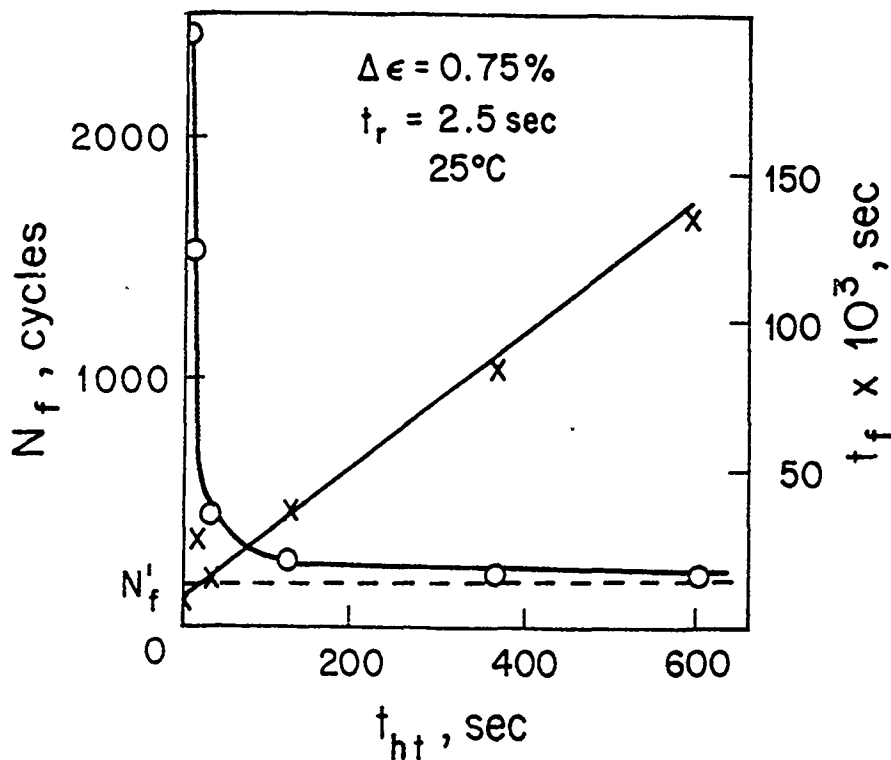
FIGURE 4. Effect of Tensile Hold Time on Fatigue
Life at 25°C. Total Strain Range 0.75%. Ramp
Time 2.5 sec.

find the limit in the fatigue life of solder. The proposed method to calculate the limit in fatigue life of solder may be used as a basis for accelerated fatigue test development.

As seen from Figure 6, grain boundary fracture is the main failure mode when a tensile hold time is introduced into the cycle. At the same strain range in no hold time tests the failure mode was mixed transgranular-intergranular. (Figure 2). Thus, tensile hold time in the cycle intensifies creep processes during fatigue of solder.

LIFETIME FORMULAE BASED ON MICROMECHANICAL APPROACH

A methodology for predicting lifetime of solder material has been derived by Zubelewicz et al (Reference 11) and it incorporates stress and strain micro-macro correlations determined at a characteristic volume ΔV of solder, and utilizes a concept of the dynamic macro-steady state of cycling. The number of cycles to failure is counted when the internal structure of solder reaches a limit for a stable behavior.
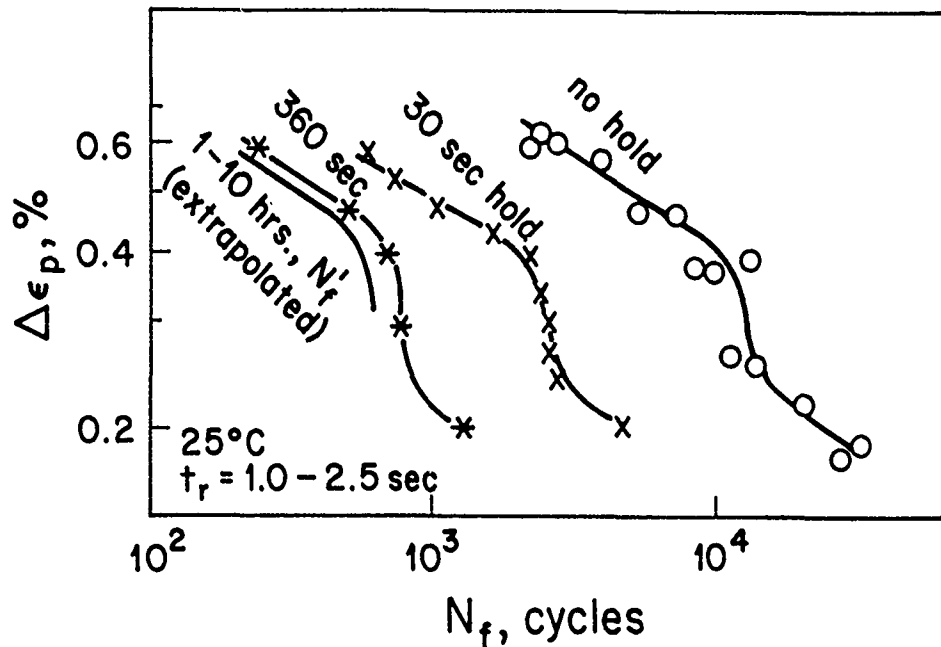
FIGURE 5. Effect of Plastic Strain Range on Number
of Cycles to Failure in Tests with Tensile Hold Time.

The stress and strain micro-macro correlations used in our
approach have been derived in general (Reference 12), which when
applied to an uniaxial strain controlled cycling appears in the
following forms:

- for tension

$$\sigma_t^{ov}(N) = \sigma_t\,\eta_t\,/\cos 2\zeta_t + \sigma_c^{ov}(N) \qquad (11_1)$$

- for compression

$$\sigma_c^{ov}(N+1) = \sigma_c\,\eta_c\,\cos 2\zeta_c + \sigma_t^{ov}(N) \qquad (11_2)$$

where the stresses $\sigma_{c,t}^{ov}$ and $\sigma_{c,t}$ as well as the parameters
$\eta_{c,t}$ and $\zeta_{c,t}$ are taken at the tensile and compressive reversals
of the N-th cycle.

The stress σ^{ov} is the overall stress defined over the
characteristic volume ΔV of solder and σ is the average microstress
smeared over the elastic matrix alone. The parameter η describes

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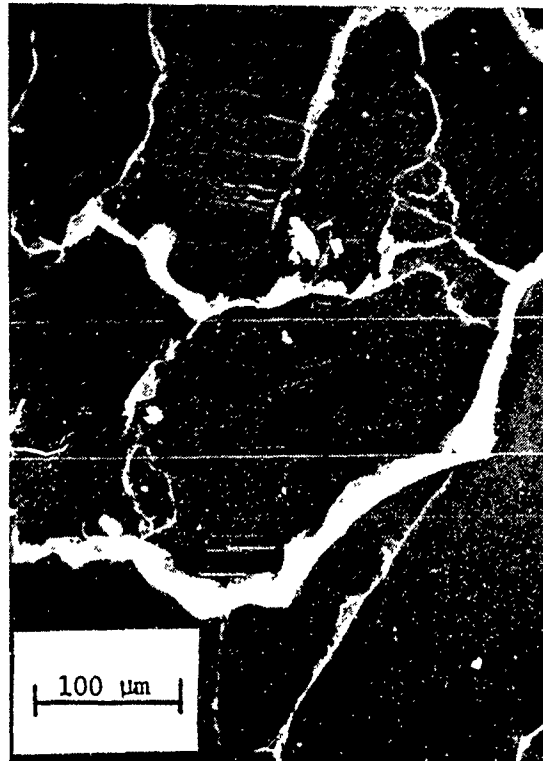
FIGURE 6. Scanning Electron Micrograph of Surface
Replica. Total Strain Range 0.75%. 25°C. Ramp Time
2.5 sec. Tensile Hold Time 90 sec. After 60% of
Fatigue Life.

hardening-recovery-damage properties and is proposed in the
multiplicative form

$$\eta = \eta_H \cdot \eta_R \cdot \eta_D \tag{12}$$

where the components indicate average hardening, recovery and damage
of solder over the characteristic volume ΔV. The parameter ζ
indicates a deviation of the average active plane (it incorporates
slip bands, active grain boundaries or microcrack surfaces) from the
direction of maximum shear stress. More specifically, compressive
stresses deviated the plane toward the stress axis, (specimen under
uniaxial load conditions), while tension rotates the plain in an
opposite direction.

Furthermore, suppose, the solder exhibits a dynamic microsteady state of cycling. The state is maintained as long as the accumulative damage (η_D) increases slowly enough to allow for a recovery of the solder's internal resistancy at each cycle.

On the other hand, cycling becomes unsteady when associated with a progressive growth of damage causing compressive reversals during the cyclic process. Therefore, <u>as long as solder is capable of recovering elastic energy at cycle reversals, such a state will be called the dynamic macrosteady state of cycling.</u>

The definition of steadiness of cycling leads to the following expression:

$$\frac{1}{2} \frac{\partial}{\partial N} [\; \Delta\sigma_t \cdot \Delta\varepsilon_t^e \; + \Delta\sigma_c \cdot \Delta\varepsilon_c^e \;] = 0 \tag{13}$$

where N indicates the number of cycles, and $\Delta\sigma_{t,c}$ is the magnitude of microstress at each cycle reversal. The elastic behavior can be considered only within the elastic matrix of the solder, thus

$$\Delta\varepsilon_t^e = \frac{\Delta\sigma_t}{E} \quad , \quad \Delta\varepsilon_c^e = \frac{\Delta\sigma_c}{E} \tag{14}$$

where E is an elastic constant. Note that $\Delta\varepsilon_t^e$ is not necessarily the same as $\Delta\varepsilon_c^e$.

All the previous derivations has been used for predicting the evolution of damage during fatigue life of solder. When substituting Equation 14 into 13, and subsequently accounting for micro-macro correlations 11, one can get

$$\eta_D = \frac{\Delta\sigma}{\sqrt{2EA}} \sqrt{\frac{\cos^2 2\zeta_t}{(\eta_{HR}^t)^2} + \frac{1}{(\eta_{HR}^c)^2 \cos^2 2\zeta_c}} \tag{15}$$

where the damage function η_D varies as a function of the internal structure ($\zeta_t, \zeta_c, \eta_{HR}^t, \eta_{HR}^c$). The parameter A is obtained after integration of Equation 13. The hardening-recovery function ($\eta_{HR}=\eta_H \cdot \eta_R$) indicates the material's ability in carrying microstresses and can be modeled as

$$\eta_{HR}^{t,c} = 1 + \kappa \cdot N \cdot \left| \Delta\varepsilon_{ov}^p \right|^n \tag{16}$$

where κ and n are material functions assuming to be identical at the

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tensile and compressive portions of the N-th cycle.

The ability of solder to resist thermomechanical cycles is limited by an increase of damage (η_D). Hence, the critical cycle N_f, considered as the end of solder's life, coincides with the critical state of the microstructure for which $\eta_D = \eta_D^{cr}$ and $\zeta_{t,c} = \zeta_{t,c}^{cr}$. Further cycling deteriorates the resistancy under the applied load conditions.

The lifetime analysis of solders incorporates the micro-macro correlations (Equation 11), evolution Equation 16 for hardening-recovery and dynamic macrosteady state of cycling (Equation 13). All of this is taken at the critical state of the internal structure of solder.

Assume that the critical configuration of solder's microstructure (η_D^{cr}, ζ_t^{cr}, ζ_c^{cr}) is already known, and the number of cycles to failure N_f is associated with this particular state. Hence, the detailed derivations of the lifetime criterion are as follows; substitute Equations 11 and 13 into Equation 15, then substitute 15 into 16 and set $N=N_f$ for $\eta_D = \eta_D^{cr}$, and $\zeta_{t,c} = \zeta_{t,c}^{cr}$. The final result is found in the following form:

$$N_f \cdot \left| \Delta\varepsilon_{ov}^p \right|^n = [\frac{B}{\eta_D^{cr}} - 1] / \kappa \tag{17}$$

where

$$B = \frac{\Delta\sigma/\tau_o}{\cos 2\zeta_c} \sqrt{\frac{1}{2}(1 + \cos^2 2\zeta_c \cdot \cos^2 2\zeta_t)} \tag{18}$$

and τ_o is the reference yield stress equal to $\tau_o = \sqrt{EA}$. The relation is identical to the Coffin-Manson law when setting B=const. The function B is dependent on the normalized stress magnitude ($\Delta\sigma/\tau_o$). The Equation 17 becomes much simpler for uniaxial tension-tension strain controlled cycling. At room temperature the average active plane follows the direction of maximum shear stress, thus $\zeta_c \cong 0$, $\zeta_t \cong 0$ and B is equal to, $B = \Delta\sigma/\tau_o$.

The lifetime Equation 17 becomes identical with the Coffin-Manson law when setting the stress magnitude $\Delta\sigma$ constant during cycling and independent on the plastic strain range. Figure 7 shows that the assumptions are quite acceptable for higher strain ranges, however, they do not apply for low strains. In other words, the Equation 17 suggests a deviation from the Coffin-Manson law at low strains as

observed by us experimentally (Figure 1).
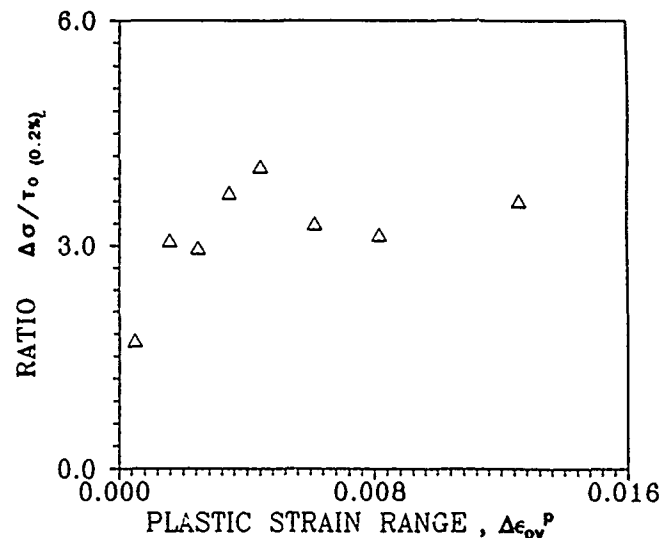
FIGURE 7. Plot of Normalized Stress Magnitude
Versus the Range of Plastic Strains.

SUMMARY

1. The Coffin-Manson relation does not hold for low-tin lead-based solder over all strain ranges below 0.75% total strain.

2. Tensile hold time has a dramatic effect on the number of cycles to failure and leads to fatigue life saturation. A simple mathematical relation between the isothermal fatigue life and tensile hold time is developed. This relation allows the determination of the limit in the solder's fatigue life.

3. A micromechanically-based model for solders reflects the non-linearity between fatigue life and strain range. The modeling shows that the variation in the failure mode and in magnitude of the stresses from varying strain range (during cyclic process) coincide with each other.

REFERENCES

1. J.H. Lau and D.W. Rice, "Solder Joint Fatigue in Surface Mount Technology: State of the Art", Solid State Technol., vol. 28, No. 10, pp. 91-104, 1985.

2. J.F. Burges et al., "Solder Fatigue Problems in Power Packages", IEEE CHMT-7, No.4, pp. 405-410, 1984.

3. L.F. Coffin, "A Study of the Effect of Cyclic Thermal Stresses on a Ductile Material", Trans. ASME, vol. 76, pp. 931-950, 1954.

4. S.S. Manson, "Fatigue: A Complex Subject - Some Simple Aproximations", Experimental Mechanics, vol. 5, No. 7, pp. 193-226, 1965.

5. H.D. Solomon, " Fatigue of 60Sn/40Pb Solder", in Proceedings of 36th Electronic Component Conference, IEEE, pp. 622-629, 1986.

6. S. Vaynman, M.E. Fine and D.A. Jeannotte, "Prediction of Fatigue Life of Lead-base Low Tin Solder" in Proceedings of 37th Electronic Component Conference, IEEE, pp. 598-603, 1987.

7. S. Vaynman, M.E. Fine and D.A. Jeannotte, "Isothermal Fatigue Failure Mechanisms in Low Tin Lead Based Solder", in Effects of Load and Thermal Histories on Mechanical Behavior of Materials, P.K. Liaw and T. Nicholas, editors, The Metallurgical Society, pp. 127, 1987.

8. S. Vaynman, M.E. Fine, D.A. Jeannotte, "Isothermal Fatigue of Low Tin Lead Based Solder", Metallurgical Transactions, vol. 19A, pp. 1051-1059, 1988.

9. L. Lawson, "Thermal Fatigue Testing of 97Pb-3Sn Solder", MS Thesis, Northwestern University, Evanston, IL, June 1986.

10. S. Vaynman, "On Fatigue Life Prediction Under Conditions of Tensile Hold", Scripta Metallurgica, vol. 21, pp. 1385-1387, 1987

11. A. Zubelewicz, R. Berriche, L.M. Keer, M.E. Fine, "Lifetime Prediction of Solder Materials", Presented at the Winter Annual Meeting of the ASME, 1988, ASME, 1988

12. A. Zubelewicz, "Overall Stress and Strain Rates for Crystalline and Frictional Materials", Submitted for Publication

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AUTOMATED SOLDER APPLICATION FOR LEADLESS DEVICES

by

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ABSTRACT

IBM Owego has investigated an alternative method of supplying solder material needed to attach leadless components in an automated environment. This technique, referred to as Solder Preforms, represents the potential to replace the solder paste process for leadless devices. Preforms are small solder objects consisting of the appropriate tin/lead ratio, and constitute the correct area/volume of solder to create the desired joint shape after reflow. Preforms have the ability to overcome many of the solder paste drawbacks because they are uniform in consistency, do not spread or slump, and are smaller in size than the equivalent amount of solder in paste form. Initial results indicate that the preform process has the potential to produce joints which visually meet all Surface Mount Technology (SMT) requirements, and far exceed the process yield expectations of the solder paste alternative, even with factory automation. This paper reviews the historical background leading to the process, the process experimentation, the automation evaluations and the anticipated merits of the solder preform technique.

INTRODUCTION

Many defense product manufacturers desire to migrate toward SMT to take advantage of increased packaging density, decreased manufacturing cost per function, and reductions in package weight to name a few. Coincidental efforts to automate electronics production have also been forefront to maximize factory performance and flexibility while minimizing product cost. However the combined aspiration to fully automate numerous SMT processes in one environment presents unique challenges to the manufacturing technologist. A case in point is the solder application process for the Navy's automated Circuit Card Assembly & Processing System (CCAPS) being developed by IBM Owego. In this automated factory endeavor, conventional solder application techniques were found to be inadequate to satisfy the system requirements, and dictated development of an approach which met the combined needs of both SMT processes and automation.

Historically, numerous techniques have been employed to provide the solder material for attachment of SMT Leadless Chip Carriers (LCCs) to circuit cards. One commonly used approach is to screen solder paste to the circuit card pads, place the LCC appropriately, and reflow the solder paste to form the electro-mechanical interconnection. Although this process is acceptable for operator assisted production, it fails to meet the demands of total automation. Design specific stencils or screens are not compatible with flexible automation architecture which demands single piece lot sizes, high part number mix, and zero set-up and clean-up. Even if a paste application process involving discrete dispensing were employed, the paste material characteristics make it difficult to provide consistent solder volume. Additionally, many technologists believe that bulbous LCC joint shapes improve the leadless component thermal life performance, particularly where the difference in coefficients of thermal expansion between the LCC and circuit card are high. To achieve these bulbous joints, large volumes of solder paste are required, resulting in numerous process problems and an increased potential for solder defects requiring rework.

IBM Owego, under direction and funding of the CCAPS contract, has investigated an alternative method of supplying solder material needed to attach leadless components in an automated environment. This technique, referred to as Solder Preforms, represents the potential to replace the solder paste process for leadless devices. Preforms are small solder objects consisting of the appropriate tin/lead ratio, and constitute the correct area/volume of solder to create the desired joint shape after reflow. Preforms have the ability to overcome many of the solder paste drawbacks because they are uniform in consistency, do not spread or slump, and are smaller in size than the equivalent amount of solder in paste form. Initial results indicate that the preform process has the potential to produce joints which visually meet all SMT requirements, and far exceed the process yield expectations of the solder paste alternative, even with factory automation. This discussion will review the historical background leading to the process, process experimentation, automation evaluations and the anticipated merits of the solder preform technique.

HISTORICAL BACKGROUND

In order to fully appreciate the value of the solder preform process, a review of the history surrounding the CCAPS solder application task is essential. The first significant item to discuss is the CCAPS requirement to have a bulbous solder joint shape for LCCs, coupled with a component to circuit card space ... sometimes referred to as a component standoff. Research from a variety of companies has shown that a bulbous solder joint shape will improve LCC thermal life performance, particularly on epoxy-glass circuit cards where the difference between the board and component coefficients of thermal expansion are high. Furthermore, development work specific to CCAPS has shown that a component standoff not only enhances the ability to achieve Mil Spec cleaning, but is required to guarantee clean product in a totally automated line like CCAPS. Additionally, there is some data which suggests that component standoff can positively affect thermal life of LCCs. In theory, the taller solder joints resulting from a component standoff may offer the ability to accept more strain before fractures in the solder occur.

The second element which had historical relevance to the solder preform activity was the CCAPS Solder Paste Discrete Dispensing Study conducted by IBM. This Solder Paste Study requires some background explanation of its own. The automated environment of CCAPS, with its single piece lot sizes and high part number mix, is not the type of environment which is conducive to design specific stencils or screens. Additionally, the set-up and clean-up times associated with single circuit card solder paste application are virtually impossible to accommodate while maintaining high equipment availability and no operator intervention. As a consequence, IBM and the Navy concluded that stencils and screens were not compatible with the CCAPS automation philosophy, and embarked on a nine month study to evaluate a solder paste discrete dispensing concept for solder material application. Lab type equipment was employed to evaluate the numerous aspects important to successful dispensing of solder paste. By the completion of the study, several major problems suggested that this technique was not ideal for CCAPS.

To discuss solder paste dispensing limitations relative to CCAPS, one must first recall the desire to have a bulbous solder joint shape coupled with a component standoff. To achieve such a joint configuration requires a substantial volume of solder paste. This volume, combined with the paste characteristics needed to facilitate dispensing, conflict with one another. A liquidous paste is desired for dispensing, however a liquidous paste will not maintain its dispensed shape well. It will attempt to seek its own level by virtue of gravity. Perhaps the terms spread or slump create a mental picture of this effect. In any case, the resulting condition usually manifests itself in a solder bridging defect after reflow. Additionally, inconsistencies in the paste material viscosity or environmental temperature can affect the dispensed volume. This results in solder joints, (potentially on the same LCC), of various sizes ... a condition which is know to adversely affect thermal life. Another problem more germane to CCAPS automation is that of nozzle clogging after idle periods, as well as the desire to be assured that the correct volume of paste is present on each circuit card pad site. Finally, IBM was not able to dispense a sufficient volume of solder paste in a single pass operation to create a quality bulbous joint. These factors, and more, led to the conclusion that discrete dispensing of solder paste would not satisfy all of the CCAPS objectives for solder application.

As an individual analyzes the drawbacks of dispensing solder paste, it is the liquidous form which manifests many of the process limitations. Obviously if a solid solder object of correct mass could be substituted for the liquidous paste, many of the process problems would theoretically be overcome. This thought process evolved into the solder preform concept for solder application.

Considering that many of the CCAPS processes to be implemented were already underway, and that a solder application process strategy was essential to CCAPS SMT, a succinct solder preform feasibility study was proposed to the Navy, commencing as soon as possible. The proposal recommended evaluating the potential for using solder preforms to meet the solder application requirements for CCAPS, and sought to define critical parameters and process windows confirmed by solder joint inspection results and mechanical fatigue testing of assemblies. Obviously it would be essential to analyze the entire process for CCAPS automation compatibility. The remainder of this paper involves a summarization of the study which was conducted, completed and presented to the Navy during 1988.

SOLDER PREFORM MASS DETERMINATION

The first phase of solder preform evaluation involves the determination of solder mass required to form a bulbous joint shape in conjunction with a component standoff. This was accomplished by computing the volume of solder contained in a typical LCC solder joint shape. First a representative sketch of the entire LCC solder joint was developed, then converted to a linear approximation to facilitate volumetric calculations. Figure 1 depicts the typical LCC joint and its linear approximation. The linear approximation was segmented into regions and formulas were developed to calculate the area of each region. Figure 2 provides an exploded view of the linear approximation used to calculate the region volumes (V1 through V6). By combining the region volumes, the LCC joint linear approximation was established and could be easily converted back to actual solder joint contour.

| Sketch | Linear Approximation |
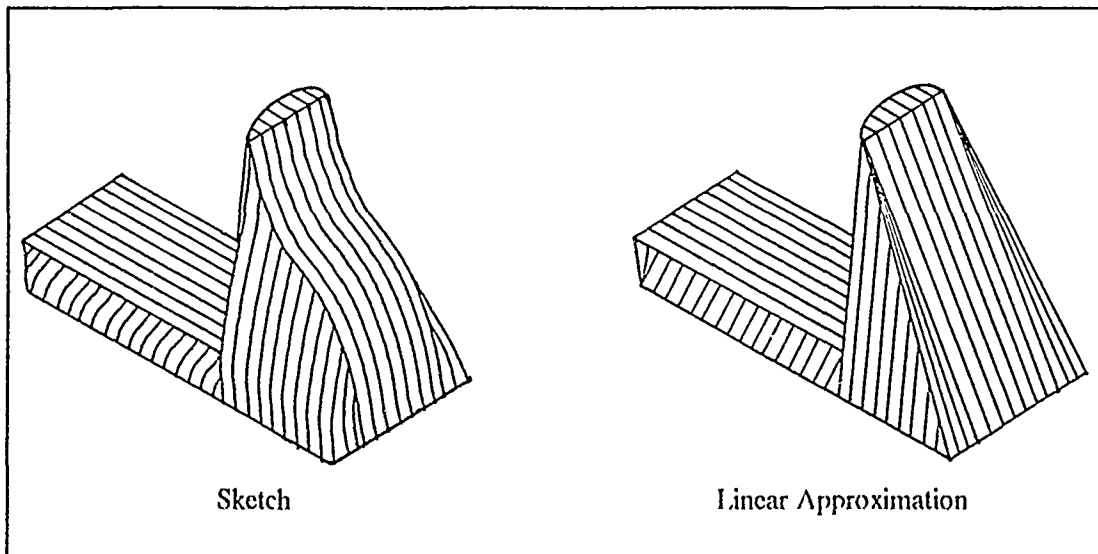
FIGURE 1. LCC Solder Joint Sketch and Linear Approximation.
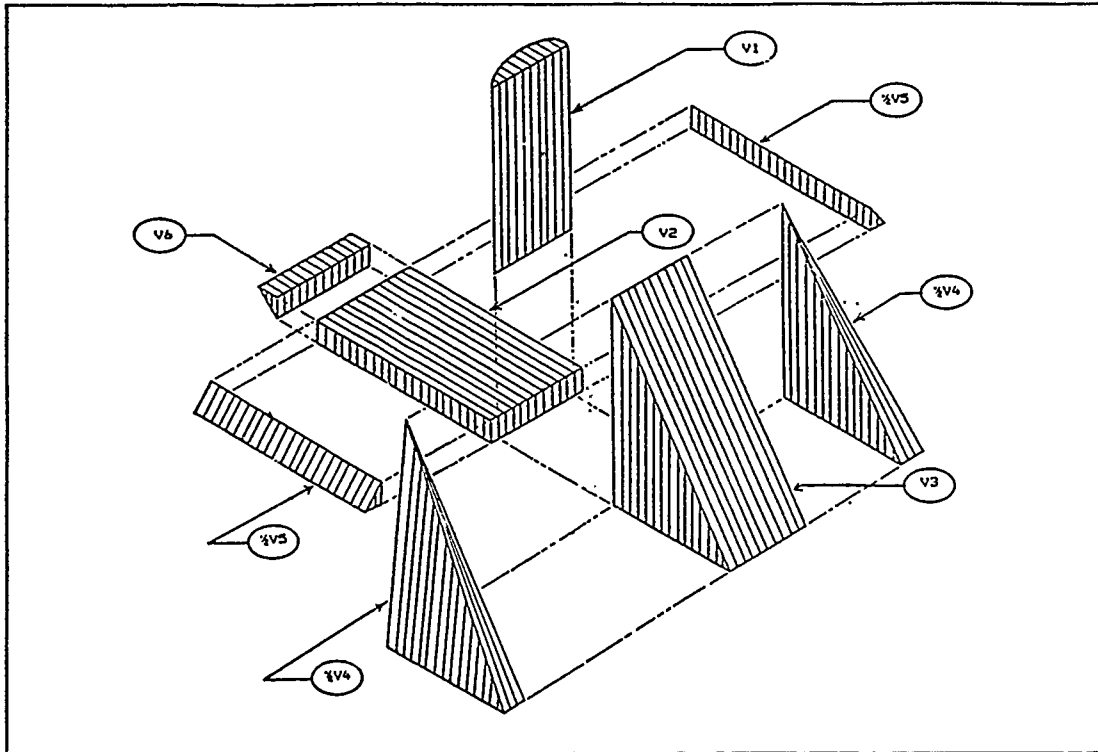
FIGURE 2. LCC Solder Joint Linear Approximation Exploded View.

In a normal production environment, solder joint shapes (either desired or resultant) can vary dependent on a number of influences. Consequently an approach was adopted for linear approximation conversion which would permit calculation of a range of solder joint shapes. This approach is referred to as the 'K' factor, which is simply a multiplier for the solder joint volume determined from the linear approximation, and is used to identify the mass of solder joints exhibiting a bulbous profile. To further explain this, the solder joint shape used to establish the original linear approximation received a K factor of 1.0. As the bulbous nature of the joint increases, the solder volume will also increase, therefore so should the K factor. This relationship was empirically tested for K factors through 1.5. CCAPS, with its bulbous solder joint expectation, would require a solder volume equivalent to a 1.3 K factor. Figure 3 provides sketches of LCC joints with the corresponding K factors for comparative purposes.

| K = 1.0 | K = 1.3 (Desired) | K = 1.5 |
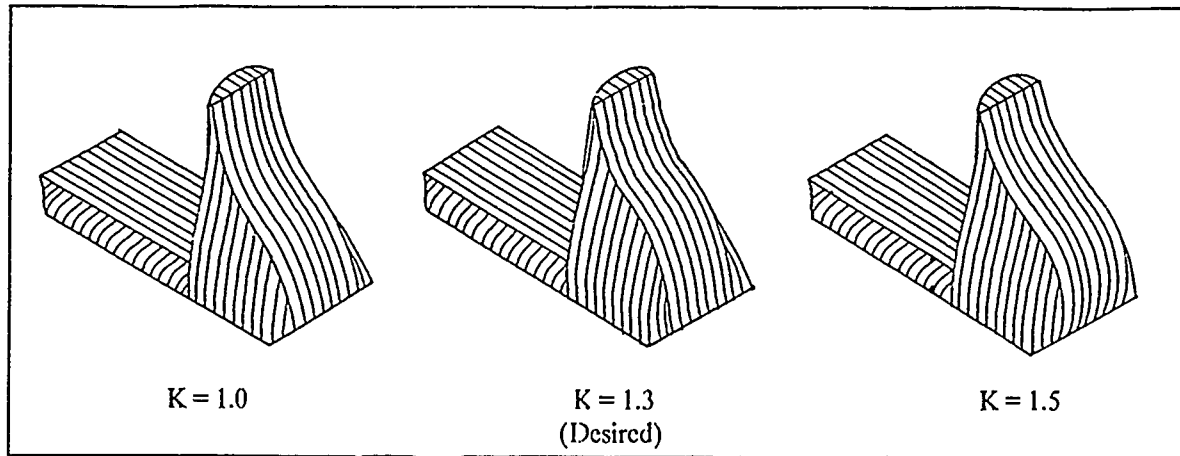
FIGURE 3. LCC Solder Joint K Factor Representations.

As was previously stated there are other variables, which affect solder joint shape, that need to be considered to determine a joint volume relative to a desired joint configuration. The thickness of any LCC component can vary between suppliers and is frequently different with the same vendor for various lead count packages. This dimension affects the LCC castellation height which consequently affects solder joint volume. Castellation width and curvature are also variables affecting joint volume. These component variables dictate that several unique solder preform masses will be required to meet the solder volume needs of all LCC devices. Since board pads and LCC s are usually pretinned, the solder thickness already present must be factored into the volume equation. Also, the length and width of board pads have an allowable tolerance which can affect joint volume on shape. And there are other variables like the component standoff height, the distance the LCC extends over the board pads, or any solder volume fluctuations permitted by the solder application process. All of these variables must be considered in order to establish LCC solder joint volume.

To assess the impact of the aforementioned variables on solder joint shape, components from 3 vendors were obtained and measured to identify dimensional variation. Additionally, IBM circuit cards were used to obtain LCC board pad variables data. Table 1 depicts the average dimension of 20 samples for each LCC size/circuit card studied. All figures are in thousandths of an inch (mils).

TABLE 1. Variables Affecting Solder Joint Volume - Average of Measurements.

Variable Name	20 I/O	28 I/O	44 I/O	52 I/O	68 I/O	84 I/O
LCC Castellation Curvature	7.7	13.7	13.4	12.8	13.5	13.6
LCC Castellation Width	17.8	19.8	21.1	20.4	20.4	21.2
LCC Castellation Heigth	36.4	37.5	46.1	57.3	53.1	53.1
LCC Solder Pad Width	23.5	22.8	23.3	23.8	23.7	23.3
LCC Solder Pad Length	48.0	46.6	44.8	45.3	48.8	49.8
Board Solder Pad Width	30.7	30.9	31.2	31.0	31.9	30.5
Board Solder Pad Length	75.9	76.1	76.1	75.8	75.2	75.4
Pretinned LCC Solder Height	1.4	1.2	1.5	1.9	1.3	1.6
Pretinned Board Solder Height	0.9	1.3	0.8	1.0	1.0	1.1

In an effort to demonstrate the potential impact of component variation on solder joint volume, note the variable 'LCC Castellation Height'. This dimension increases about 40% from the low I/O packages to the high I/O. This type of change will affect the solder joint configuration unless more solder is added. In the next chart, the standard deviation of the 20 sample measurements is displayed.

TABLE 2. Variable Affecting Solder Joint Volume - Standard Deviation of Measurements.

Variable Name	20 I/O	28 I/O	44 I/O	52 I/O	68 I/O	84 I/O
LCC Castellation Curvature	0.77	1.33	0.33	0.69	0.57	0.73
LCC Castellation Width	0.41	0.26	0.35	0.44	0.20	0.27
LCC Castellation Heigth	0.22	1.07	1.21	0.86	0.68	0.69
LCC Solder Pad Width	0.18	0.37	0.20	0.26	0.12	0.26
LCC Solder Pad Length	0.81	0.43	1.53	1.48	0.99	0.58
Board Solder Pad Width	0.56	0.38	0.72	0.54	0.48	0.37
Board Solder Pad Length	0.77	0.97	0.76	1.04	1.25	0.48
Pretinned LCC Solder Height	0.21	0.32	0.27	0.18	0.26	0.31
Pretinned Board Solder Height	0.28	0.31	0.18	0.21	0.27	0.32

After the variables data was obtained, a computer model was developed to determine the most sensitive variables as well as the solder joint shape distribution resulting from random variable selection. The computer analysis considered 2500 unique data combinations extracted from the data previously presented. The analysis provided assurance that a solder preform mass could be determined for each size LCC component which would consistently yield an accept-

able joint shape, regardless of the other variables involved. Utilizing the solder joint volume calculations, a theoretical solder preform mass was determined for each LCC size. Through a parallel test effort, the optimum preform footprint was also established. Once the mass and footprint size of the preforms were established, selection of preform thickness to obtain the correct mass was straightforward. Table 3 displays the theoretical volume calculations, the preform sizes and their resultant actual mass, and the computer analysis shape distribution for the various LCC sizes. The data suggests that 5 unique solder preform thicknesses would be required to facilitate bulbous joint shapes on the 6 LCC sizes.

TABLE 3. Solder Preform Mass Determination Summary.

LCC I/O	THEORETICAL MASS (mg)	SHAPE (mils)			ACTUAL MASS (mg)	JOINT SHAPE %		
		Ln	Wd	Th		1.2	1.3	1.4
20	3.43	65	30	12	3.2	56	44	0
28	3.68	65	30	13	3.5	57	43	0
44	4.52	65	30	17	4.5	8	87	6
52	5.12	65	30	19	5.0	17	83	0
68	4.74	65	30	18	4.8	1	89	10
84	4.61	65	30	18	4.8	0	73	27

Once the desired preform dimensions had been determined, larger quantities of preforms were obtained from solder suppliers. LCC solder joints were created in larger quantities and visually inspected to empirically verify the shape distribution cited by the computer analysis. Additionally, the mass consistency of supplied preforms was evaluated by selecting 100 preform samples for each preform mass and individually weighing each sample. It was determined that the mass consistency typically fell with 5% of the ordered value. Evaluation of the efforts to determine solder preform mass suggested that preforms could be obtained and would result in solder joint shapes which were very uniform regardless of LCC size or dimensional variations. The next step was to investigate the aspects of providing the flux necessary to achieve quality bulbous joints.

FLUXING & REFLOW EVALUATIONS

Anyone conversant with soldering realizes that flux is usually an integral part of the soldering operation. It's purpose is to remove surface oxides and facilitate wetting of the solder to the surfaces to be joined. Relative to solder preforms, flux provides another function. It holds the preforms in place until reflow. Flux generally has a material characteristic of being sticky or tacky. If a layer of flux is deposited on a circuit card, the flux acts something like fly paper. Almost anything placed on the flux will be less apt to move than if the flux wasn't there.

This condition allows preforms to be placed on the circuit card and the location secured by the tackiness of the flux. After the preforms have been located, the component will be placed on top of the preforms. By applying a second coating of flux on the top surface of the preforms prior to component placement, the components will also be held in place, (to a certain extent), by the tackiness of the flux. More detail about this will be discuss in the preform movement section of the report.

In the two-pass flux application concept, the first pass holds the preform, the second pass holds the component, and both passes promote good solder bonds. A design constraint for the flux application process was brought about by the standoff function. The standoff material, which will be deposited after solder application but prior to component placement in the CCAPS flow, cannot tolerate the presence of flux on the standoff board site. Consequently, the flux application process must be capable of selectively locating the flux on the circuit card pad area, while not permitting flux to be deposited inside this pad outline. Lastly, the flux application method must be compatible with the CCAPS automation strategy. A relatively consistent thickness of flux must be automatically deposited within the solder application machine, taking into account variations ranging from flux viscosity to circuit card design. Although several fluxing techniques were found to meet these CCAPS requirements, an air brush applicator seemed to provide the most consistent results. The air brush employed for testing was of the variety commonly used to paint customized artwork on automobiles and trucks.

Because CCAPS is intended to be compatible with both Infra-Red and Vapor Phase reflow techniques, the feasibility of creating quality solder joints using preforms had to be evaluated using both reflow approaches. As was expected, both methods consistently yielded solder joints of equal quality. Table 4 identifies the basic parameters determined via the study. The data is not considered optimized, but more an excellent starting point for parameter definitization.

TABLE 4. Approximate Reflow Parameters for Preforms.

ZONE	VAPOR PHASE	INFRA-RED
Preheat	120 seconds @ 80-90°C	180 seconds @ 75-85°C
Reflow	45 seconds @ 205-215°C	120 seconds @ 205-215°C
Cooling	20 seconds of solvent spray (8°C/second)	60 seconds of impinged air (.75°C/second)

The cooling data reflected in table 4 is not necessarily specific to either reflow method, and requires some further explanation. The rate at which solder solidifies has been proven to have an influence on the metallurgical grain structure of the solder joint ... and consequently the thermal life performance. IBM, through its own funding, has investigated inducing rapid solder solidification by changing the cooling profile of the reflow machine. The physical attributes of

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the solder joint are not affected, however improvements in thermal life can be substantial. This topic will be discussed in more detail in the fatigue testing portion of the paper.

PLACEMENT/MOVEMENT EVALUATIONS

Solder preforms, from a dimensional perspective, do not differ greatly from the smallest SMT capacitors marketed today. This thought process suggests that capacitor placement equipment could be used to place preforms. Since a typical LCC type circuit card has numerous component sites which would require a substantial amount of preform placements, a high-speed placement machine would be advantageous. Capacitor placement equipment, like chip shooters, involve a turret head design to achieve over 12,000 placements per hour and are the basis of the desired preform placement rate. In terms of component sites, this would equate to over 270 44 I/O LCC sites per hour.

Testing has been conducted to evaluate the placement accuracy of solder preforms in order to achieve a low solder touch-up process. Although accuracy requirements are dependent on circuit card and component design, flux volume, and operator handling, preform placement accurate to $+/-.004''$ is desired. Additionally, $+/-10$ degrees rotational accuracy is required. The fact remains that preforms exhibit good self-centering tendencies, often pulling back to the solder pad even when misplaced.

Solder preforms, by virtue of their size and the tackiness of the flux, do not tend to move once placed. Before this phenomenon was understood, various means to hold the preforms in place were investigated. One technique, which proved feasible, was ultrasonic tacking of the preforms to the circuit card pad. This approach created a physical bond between the two surfaces which could withstand substantial force, yet involved precious process time to accomplish. It was deemed technically feasible, but was not required because flux tackiness was found to be sufficient to hold the preforms in place.

Another element to the movement equation is the component resting on top of the preforms. The flux tackiness, coupled with the surface contact area with solder preforms, attempts to maintain the component's location until the solder connection is made. A portion of the study sought to evaluate the force necessary to dislodge the component, (or preform), from its placed location and equate this to an actual CCAPS production environment. Using a vibration tester, it was determined that a pulse equivalent to 5 G, laterally or vertically, would not adversely affect the component location. Additionally, no component movement resulted from a continuous pulsing of 0.4 G for 30 seconds, at which time only the largest component showed movement. To verify that the CCAPS material handling system would not cause preform nor component movement, testing on actual MATS robots was conducted. After repeated handling of circuit cards by the robots, the preform and component locations remained within acceptable limits.

SOLDER JOINT MECHANICAL FATIGUE TESTING

In order to understand the ramifications of the solder preform process on LCC thermal life, testing was conducted. The thermal cycling tests typically employed to quantify thermal life are extremely time consuming, especially if chamber space is limited. Consequently, mechanical fatigue testing was chosen to obtain more real-time data which indicated the trend of solder joint life with preforms. Figure 4 depicts the apparatus used to conduct the mechanical testing. Test specimens consist of a specially designed epoxy glass coupon, .070″ thick with a copper layer for reinforcement. *Mounted on the test coupon is a functional 44 I/O LCC module with 22 LCC solder joint connections. These connections involve leads on 2 opposite sides of the LCC, consisting of bulbous solder joint shapes exhibiting a 5 mil standoff. One side of LCC solder joints are then potted in epoxy and the test coupon is mounted in the test fixture. The side support portions of the coupon are cut so that mechanical deflections will properly displace the unrestrained LCC solder joint assembly. A total deflection of one-half mil and a test rate of 6 minutes per cycle were employed, providing fatigue test results in generally less than a week. The test coupons were electrically monitored to establish a set .02 ohm failure point.
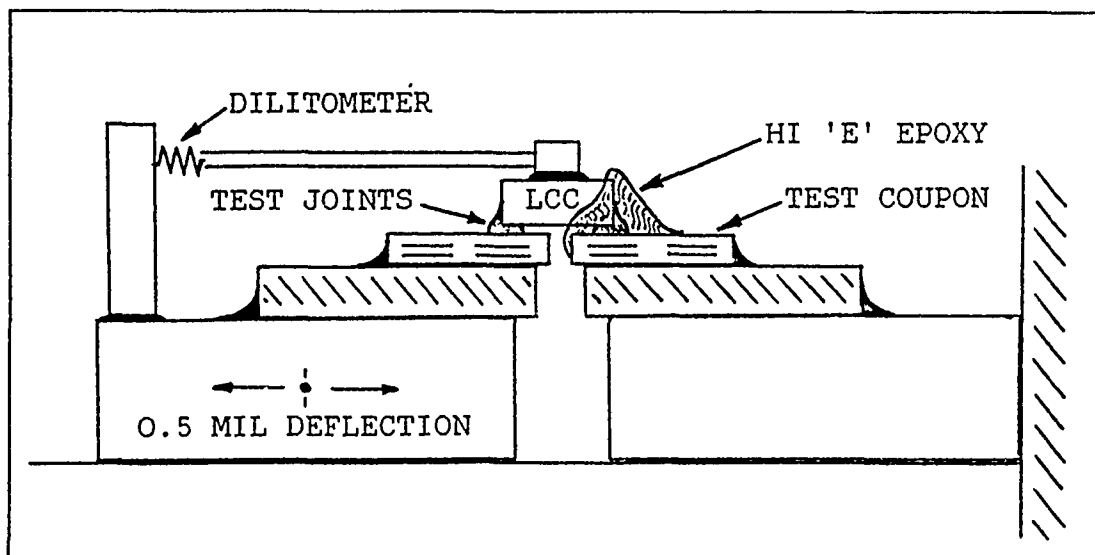
FIGURE 4. Mechanical Fatigue Tester.

The test matrix involved several variables including two distinct solder joint shapes, ('C' and 'D'), and two cooling profiles for vapor phase reflow. The two joint shapes correlate to K factor as follows: 'C' corresponds to a K factor of 1.15 and 'D' equates to 1.3. The rationale

for two solder joint configurations was to provide insight to the premise that more bulbous joints equate to increased joint life. The different cooling profiles, referred to as 'conventional' and 'rapid', were introduced to permit the test results to be compared with an existing database of LCC joints fabricated using solder paste which was previously tested by IBM. The justification for two cooling profiles primarily involves the potential for improving LCC fatigue life, offset by the fact that certain current military specifications do not permit forced cooling of solder joints. Some background information on rapid cooling is summarized in the next paragraph.

Various studies have been conducted which indicate that a finer alloy solder joint grain structure results in LCC fatigue life improvement. This is based on the findings that solder joint deformations in thermal cycling normally take place along the grain boundaries in the solder. The coarse or large solder grain structure, which is created by conventional reflow cooling profiles, will create faster fatigue damage along the large grain boundaries. Additionally there can be excessive precipitation and growth of lead rich phases during this slow cooling. These concentrations of soft and weak lead phases are prone to crack propagation under fatigue stress. Decreasing the solder solidification time will reduce the solder grain size, minimize the potential for lead rich phases, and consequently improve the solder joint fatigue life. Carefully controlled forced cooling of solder joints has been found to be a feasible method to reduce grain size. This rapid cooling concept was included in the solder preform fatigue test matrix to realize the potential improvement on LCC fatigue life.

Table 5 displays results from the mechanical fatigue testing of LCC solder joints fabricated using solder preforms. A total of 13 specimens were prepared and reflowed with the vapor phase technique previously described. The apparatus which accomplishes rapid cooling of the product was turned off to achieve the conventional cooling test specimens. The mechanical fatigue testing data suggests that a more bulbous joint shape combined with rapid cooling will provide the optimum solder joint fatigue life.

TABLE 5. LCC Solder Joint Mechanical Fatigue Test Comparison.

COOLING	C JOINT	D JOINT
Conventional (< 2° C/second)	177	290
Rapid (> 8° C/second)	593	1180

The solder preform mechanical fatigue results were also compared to an existing database to provide additional insight into the potential merits of preforms. IBM's Roger Wild, in his report on "Factors Affecting LCC Solder Joint Fatigue Life II", utilized mechanical fatigue testing to compare the fatigue life of three techniques. Hand soldered joints, which cool very rapidly due to the circuit card acting as a heat sink, were prepared with a 'D' joint shape and had a .004" component standoff. Secondly, solder joints created with solder paste, reflowed

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using vapor phase combined with rapid cooling, were manufactured to the same configuration. Third, solder paste combined with a standard (conventional) cooling profile were employed to connect LCC s which were then conformally coated with a .001" thick Paralene coating. There are not a high number of tests in each category however what is shown in Figure 5 is believed reasonably accurate.
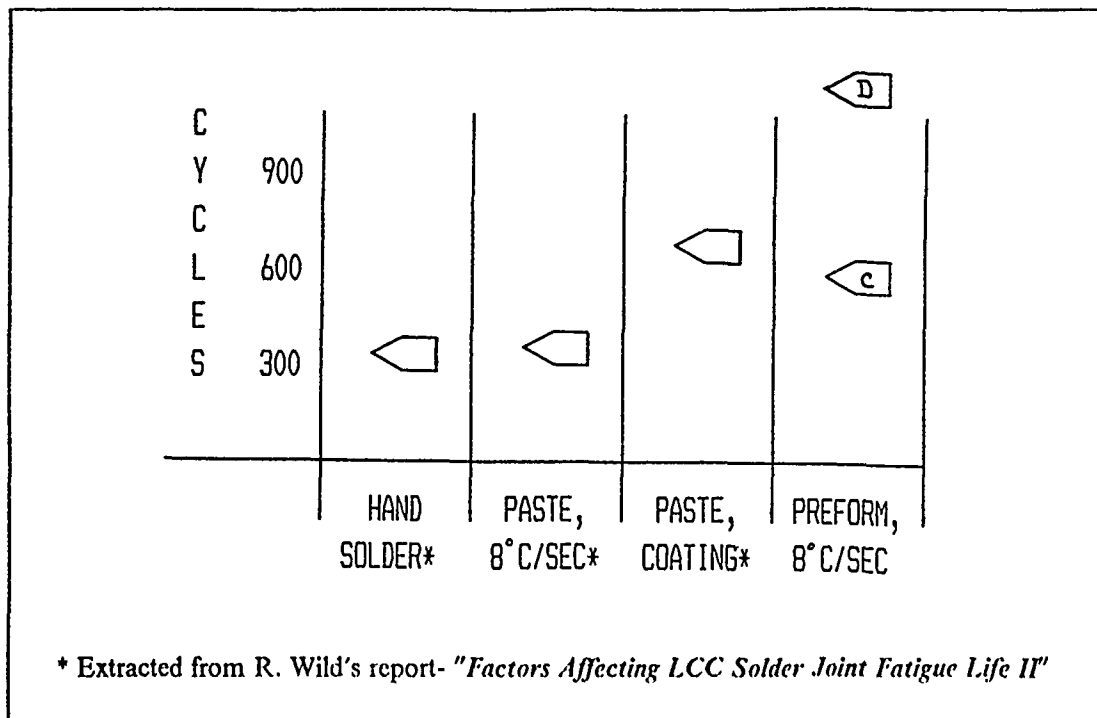
FIGURE 5. LCC Solder Joint Mechanical Fatigue Test Results.

Examining the mechanical fatigue test results of solder preforms to the historical data provided by Roger Wild's report, any differences must be discussed. Obviously, the solder preform study utilized solder preforms to provide the media for interconnection while the others involved solder paste. Additionally, the preform study incorporated a .005" standoff as opposed to .004" for the other data. These are believed to be the only differences of any potential significance. The solder preform study fatigue testing results, consisting of 13 test samples, suggests that the combination of solder preforms, bulbous joint shape, 5 mil standoff and rapid cooling represent the potential to dramatically improve LCC fatigue life on epoxy-glass circuit cards. Thermal fatigue testing to verify these results is currently underway.

AUTOMATION ASSESSMENT

Based on the process feasibility investigations, it is evident that solder preforms are a viable technique for supplying the solder to connect LCC components to circuit cards. But this alone does not substantiate that the process can be automated in a CCAPS environment and is flexible enough to satisfy CCAPS requirements. As a consequence, the automation assessment portion of the study considered if the preform processes could be accommodated without manual intervention.

The fluxing requirements provide only a minor challenge for automation design. Both syringe dispensing and air brush techniques have the potential to meet all the needs. Also, a sponge applicator cannot be ruled out, although some development would probably be required to obtain the optimum sponge material. Preform placement tolerances should also be relatively easy to meet. Not only are the placement limits within the realm of chip shooters, but the possibility exists to serially link more accurate but slower placement equipment. For Owego's implementation, no more than 10 unique preform sizes would be required for the leadless component product set, which includes LCCs and capacitors. Preform suppliers have the capability to meet the mass consistency requirements with almost no extra effort. The preforms can be packaged in 8mm tape to facilitate feeding to the placement apparatus, or can be punched from solder ribbon immediately prior to placement. Any number of placement devices can be employed to insure accuracy, and the turret style head also offers a high speed capability. At a minimum, machine vision could be incorporated to verify preform placement however this is not a requirement. Preforms can be used in either Vapor Phase or Infra-Red reflow equipment, an important aspect for CCAPS flexibility. The reflow subsystem, as well as LCC or capacitor mounting equipment, is totally independent of the solder application machine. This means that solder preforms for solder application are not dependent on the rest of a CCAPS line, but can be substituted for any existing solder application scheme.

SUMMARY

Using the experience gained from the solder preform study, IBM believes that preforms are not the optimum approach for solder application for .025" pitch componentry. Dependent on component type and circuit card design, .040" pitch is a reasonable limit for application of the solder preform technique. The rationale is that preforms become too small to effectively handle for fine pitch componentry. Additionally, preforms do not permit simultaneous double-sided board soldering. Placing preforms and components on both sides of a circuit card will result in the bottom side components falling off before reflow. The concept of using adhesive to hold the components in place does not apply because the preform height before reflow is greater than the desired component to board spacing after reflow. Solder paste overcomes this condition by permitting the component to be pressed into the paste down the the desired spacing.

There are many technical advantages to solder preforms on leadless componentry. First, preforms permit a single pass creation of the desired solder shape with a range of component standoff heights. Bulbous solder joint configurations are no problem with solder preforms. Based on data collected during the study, it is expected that less than 2% of the solder joints made using preforms will need to be touched-up in a manufacturing process. This takes into account variations in incoming product quality as well as normal process perturbations. Within the same process, solder joints for capacitors can be fabricated. To date, no capacitor solder joints have been thermally tested, however visually they meet all weapons spec criteria. Preforms are compatible with either of the commonly used SMT reflow methods, although the majority of the study was conducted using vapor phase due to convenience. The technology exists to automate the solder preform operations. In fact, IBM is currently involved with the development and build of a machine which will satisfy the solder application requirements discussed in this paper.

As defense product manufacturers migrate toward SMT and implement factory automation to reduce cost and enhance flexibility, certain processes will need to be modified. Additionally, product design to accommodate these implementations will also change driving new requirements on the process. IBM's experience with CCAPS suggests that solder application is one such process which has to undergo major revision to permit automation ... and that solder preforms as the vehicle is the correct approach given the process constraints. There is high confidence that solder preforms will not only meet the requirements of CCAPS automation strategy, but will also improve the ability to create quality solder joints on LCC devices and enhance LCC solder joint thermal life.

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NEW ADHESIVE MATERIALS FOR PWB ASSEMBLY

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ABSTRACT

This paper will discuss the properties and uses of three types of preformed elastomeric sheet adhesive materials as alternatives to the popular liquid or frozen sheet adhesive types. Applications covered include hybrid circuit mounting, flat pack mounting and stand-off, heat sink attachment to components, and heat sink attachment to printed wiring boards.

INTRODUCTION

Many needs exist in the area of electronic assembly for a wide variety of materials both for discrete component attachment and for PWB attachment to heat sinks. Currently available materials include cyanoacrylates, UV curable acrylics and urethanes, and filled silcone RTV's, as well as filled and unfilled epoxies in liquid and frozen sheet preforms. This research focused on alternative materials which address some of the shortcomings of these systems in certain electronic assembly applications.

Specifically, materials were looked at which can be manufactured into a semi-solid sheet form in a desired thickness which can be easily handled and form a flexible bond. This paper will detail the properties and applications of three types of materials: a 2-sided pressure sensitive adhesive tape for component mounting and stand-off; a 2-sided thermally conductive pressure sensitive adhesive tape for component mounting and heat transfer; and a thermally conductive silicone elastomer sheet which can be used to form a bond between dissimilar materials.

TYPE I - COMPONENT MOUNTING PRESSURE SENSITIVE ADHESIVE TAPE.

COMPOSITION:

* Core material - Polyimide film, 1-3 mils thick.
* Adhesive layers (top and bottom) - Heat activated polyacrylate copolymer pressure sensitive adhesive; approx. 2 mils each side.

Physical data on a composition of this type using 1 mil film is shown in Table 1.

ADHESIVE CHARACTERISTICS:

* High tack for good "quick-stick" to component and board surface.
* Heat activatable properties include increased bond strength, resistance to fluxes and cleaning solvents, and low outgassing properties.
* Easily removable for rework even after heat setting.
* Non-rigid (T_g = -40°C) yet non fluid. (crosslinked elastomer)
* Long shelf life (up to 1 year).

FILM CHARACTERISTICS (polyimide):

* Dimensionally stable even at soldering temperatures.
* Solvent resistant.
* High dielectric strength.

TABLE 1. - Properties of a 5 Mil Type I Composition.

Adhesive thickness (in)	.002 each side
180° peel adhesion (oz/in)	
- to steel	63
- to copper	50
- to anodized aluminum	65
- to circuit board (FR-4)	60
Lap shear strength, steel (psi)	225
Bond strength to circuit board (psi)	
- at 23°C	113
- at -25°C	8
- at -55°C	3
- at 200°C	40
Thermal conductivity	
(Cal/°C cm sec x10³)	.85

All adhesive properties are after a 5 minute heat set cycle at 175°C.

USES AND APPLICATIONS

Compositions of this type are prepared by casting the adhesive layer from solution on a continuous web of the core material, passing it through an oven to remove the solvent, and winding it up in roll form with a controlled differential release liner. The web is then reversed and adhesive is cast on the reverse side of the film. Again, the web is passed through the oven and wound into roll form. The resulting tape can then be processed into finished form by slitting into precise width and die cutting into small squares. Figure 1 illustrates one concept for dispensing and applying precut squares of adhesive film to the bottom of SMT components using a pick-and-place robot.

The use of an adhesive in precut film form lends itself well for positioning components with flat bottom surfaces prior to soldering. It is especially useful for larger, multi-leaded

components to prevent accidental movement prior and during the soldering process. To facilitate rework, it was found that peel adhesion should be limited to 50 oz/in. It should be noted that the composition chosen for the initial study in Table 1 was judged to be somewhat difficult to rework. The thickness of a single layer of Type I or II is limited for all practical purposes to a maximum of 10 mils by film flexibility and by the optimum adhesive layer thickness of 2 mils. This was found to provide the best balance of dimensional stability, conformability, and adhesion.

In the case of components with a high standoff height, this system is easily adapted by laminating several layers of tape together. Figure 2 shows the mounting of an SOIC flat-pack component with a 25 mil standoff using a laminate of 5 layers of a 5 mil thick construction. In this application, it was noted that the use of the pressure sensitive laminate resulted in a slight positive pressure exerted by the leads into the solder paste.

TYPE II - THERMALLY CONDUCTIVE PRESSURE SENSITIVE TAPE FOR COMPONENT MOUNTING/HEAT TRANSFER.

COMPOSITION:

* Core material - Alumina filled polyimide film 1-3 mils thick.
* Adhesive layers (top and bottom) - Alumina filled, heat activated polyacrylate copolymer pressure sensitive adhesive; approximately 2 mils on each side.

Data on compositions using 50 and 60% by volume of alumina in the adhesive are shown in Table 2. Composition B was found to be easier to rework and had better heat transfer properties.

ADHESIVE CHARACTERISTICS:

* The base adhesive resin used to make Type I was also used to make the Type II formulations. Adding filler lowers the inherent adhesion levels while more than doubling the rate of

heat transfer through it. Table 3 shows the effect of heat setting on both the Type I and II in terms of bond strength and solvent resistance.

FILM CHARACTERISTICS:

* Adding filler to the polyimide film (commercially available) increases thermal conductivity while slightly lowering dielectric and mechanical strength. Other properties are similar to unfilled polyimide.

TABLE 2. - Data on Type II Constructions.

	A	B
* 180° peel adhesion (oz/in)		
- to steel	61	41
- to FR-4 board	37	29
* Bond strength (psi)		
- to steel	112	39
- to FR-4 board	73	24
* Lap shear to steel (psi)	224	208
* Thermal resistance (°C/watt in²)	.40	.30
* Thermal conductivity (Cal/°C cm sec x 10³)	1.7	2.6

Construction A: 50%; B: 60% (alumina, by volume in adhesive)

TABLE 3. - Effect of Heat Setting on Environmental Resistance of Types I and II.

	Type I	Type I
* Bond strength (psi)		
- at 23°C, to steel, heat set	111	39
- " " , to steel, not heat set	66	27
- " " , to FR-4 board, heat set	113	24
- at 200°C, to FR-4 board, heat set	40	72
- at -55°C, to FR-4 board, heat set	3	1
- to FR-4 board, heat set, 15 min over boiling Freon TMS vapor	113	46
- to FR-4 board, not heat set, 15 min over boiling Freon TMS vapor	68	10

Heat setting also enabled both types to pass NASA outgassing requirements of 1.0% TML and 0.1% CVCC.

Heat set cycle: 5 min at 175°C

USES AND APPLICATIONS:

Compositions of this type are prepared in the same manner as Type I compositions. The adhesive was prepared by pre-wetting the alumina powder in solvent in a high speed mixer, then adding the adhesive resin solution slowly to the mixture during agitation.

Type II adhesive tapes can be fabricated in the same manner as Type I tapes. Parts can be die cut to shape or cut from a roll. Conventional die cutting can be done, as in the case of Type I materials, or laser die cutting can be used in the case of small parts.

Type II compositions can be used in place of liquid or frozen film adhesives to mount heat sensitive components to heat sinks. Figure 3 shows a typical application: mounting a heat sink to the top of a large DIP component. Other applications include mounting DIPs to heat rails, mounting heat sinks to the top of pin grid arrays, mounting ceramic hybrid boards in metal cases, heat sinking of chip carriers, and attaching TO-220

packages without hardware. Figure 4 depicts a concentrator solar cell bonded to a copper heat spreader with Type II adhesive.

TYPE III - THERMALLY CONDUCTIVE SILICONE ELASTOMER PREFORM USED TO FORM COMPLIANT BONDS.

COMPOSITION:
* VMQ Type general purpose silicone polymer filled primarily with alumina and zinc oxide to different levels with 2,4-DichloroBenzoyl Peroxide used as the catalyst. This gives good crosslinking at $110°$ to 125°C in under 5 minutes.

The conductive fillers and peroxide catalyst were incorporated into the polymer matrix using a 2-roll mill and thoroughly blended. ASTM test slabs were prepared of different compositions. Table 4 lists the physical properties of two compositions, one compounded for higher strength, the other for high thermal conductivity. Both have a very low modulus of elasticity especially when compared to a thermally conductive epoxy.

TABLE 4. - Physical Properties of Cured Elastomers.

Cure cycle: 5 min @ 120°C.

PROPERTY	Compound A	Compound B
* Specific gravity (g/cc)	1.6	2.6
* 50% modulus (psi)	110	170
* 100% modulus (psi)	130	150
* Tensile modulus (psi)	750	250
* Dynamic modulus (psi)	1450	1900
* Ultimate elongation (%)	450	300
* Brittle point (°C)	-73	-73
* Thermal conductivty (Cal/°C cm sec x 10^3)	1.3	3.8

Compound A: 14% by vol. zinc oxide.
Compound B: 46% by vol. alumina/zinc oxide blend.

BONDING PROCEDURE:

Since these compounds are not adhesive by nature, a primer must be used to promote adhesion to various surfaces. Acceptable primers for this system include General Electric SR-500, Dow Corning DC-2260, and Lord Chemical Chemlok 607. The SR-500 gives a slight surface tack to the surface which aids in the wet-out of the elastomer to the surface and facilitates easy removal of the carrier film. SR-500 also provides a "repairable" level of adhesion compared to the other two. All primers performed well in thermal cycling from -55° to +125°C.

The silicone compounds were sheeted out to a preform thickness of .008" to construct the lap shear tests. This simulates the most demanding application since the strain rate for any given TCE differential is inversely propotional to the thickness of the bond. The silicone was pressed into contact with the primed metal surface in a manner which excluded trapped air. The carrier film was then removed exposing the second surface. Primed circuit board laminate material was then pressed on top of the silicone surface and the whole assembly placed in a nylon film vacuum bag. The assemblies were then cured under 25" Hg vacuum for 15-25 min. at 120°C (depending on the mass of the assembly).

The following constructions were evaluated for compatability:

* FR-4 to anodized aluminum
* Polyimide/Kevlar to copper/invar/copper
* Polyimide/Kevlar to anodized aluminum
* Alumina ceramic to anodized aluminum
* PTFE/copper laminate (sodium etched) to anodized aluminum

Table 5 lists lap shear results for Compound B (above) between polyimide/Kevlar and anodized aluminum at different temperatures.

TABLE 5. Lap Shear Tests on Highly Filled Type III Material Between Polyimide/Kevlar Laminate and Aluminum.

Bond thickness: .008". Cure cycle: 20 min at 120°C under 25" vacuum. Primer: SR-500 on both surfaces.

* Lap shear (psi) at		
	2 3°C	139
	130°C	88
	-65°C	394

USES AND APPLICATIONS:

Type III material is designed for bonding fully assembled printed wiring boards to heat sinks where a compliant bond which absorbs the strain induced by different rates of thermal expansion is desired. It can be used very thin (.008") in the case of surface mount boards with flat bottom surfaces or up to .060" thick in the case of through-hole boards. It can also be used without primer as a "potting compound" between the component side of the board and a heat sink or chassis surface. Figures 5-7 illustrate these applications.

Pick and Place Head

Component

Die Cut
Adhesive Pad

Notched Release Liner

Take Up Spool

Position Sensor/Touch Down Pad

Roll Stock with
Pre-Cut Adhesive Pads
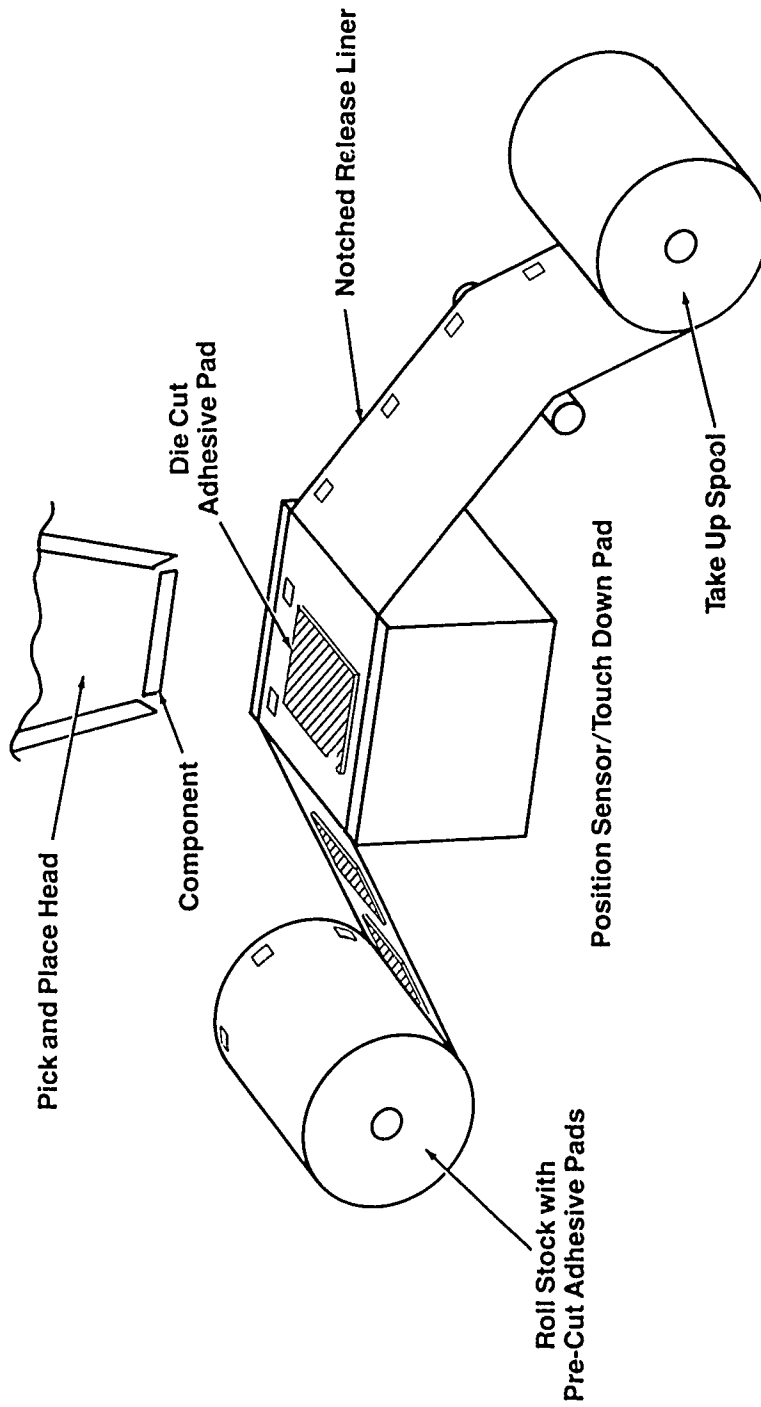
FIGURE 1. — Concept for Application of 2-sided
Pressure Sensitive Adhesive Using Pick-n-Place Equipment.

Detail A

Component

Board

Pressure Sensitive
Acrylic Elastomer

Polyimide Film

.025"

Printed
Wiring
Board

Gull Wing Component

Tape Laminate — 25 mil
(See Detail)

A
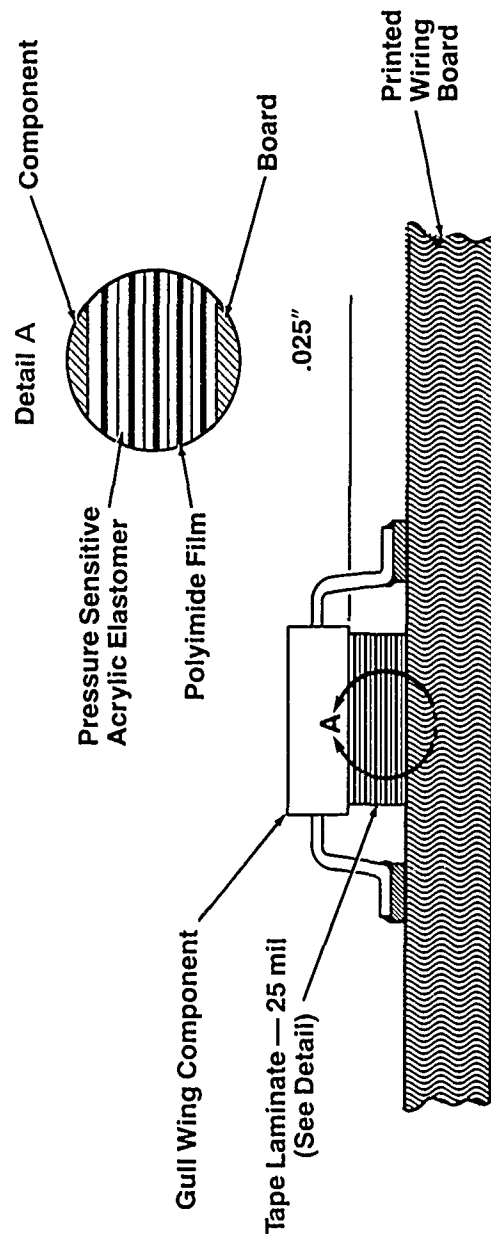
FIGURE 2. — Mounting of a High Standoff Component
Using a 5-Ply Lamination of Type I Tape.

Heat Sink

Thermally Filled
Adhesive Layers (2)

Thermally Filled
Polyimide Film
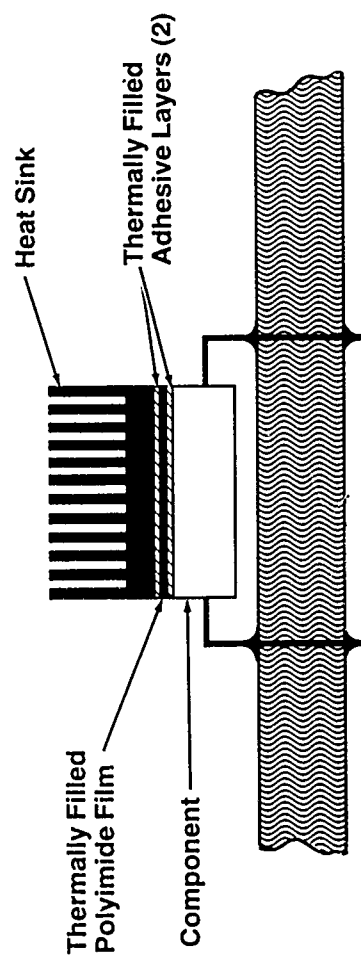
Component

FIGURE 3. — Heat Sink Mounted on Top of DIP Component.
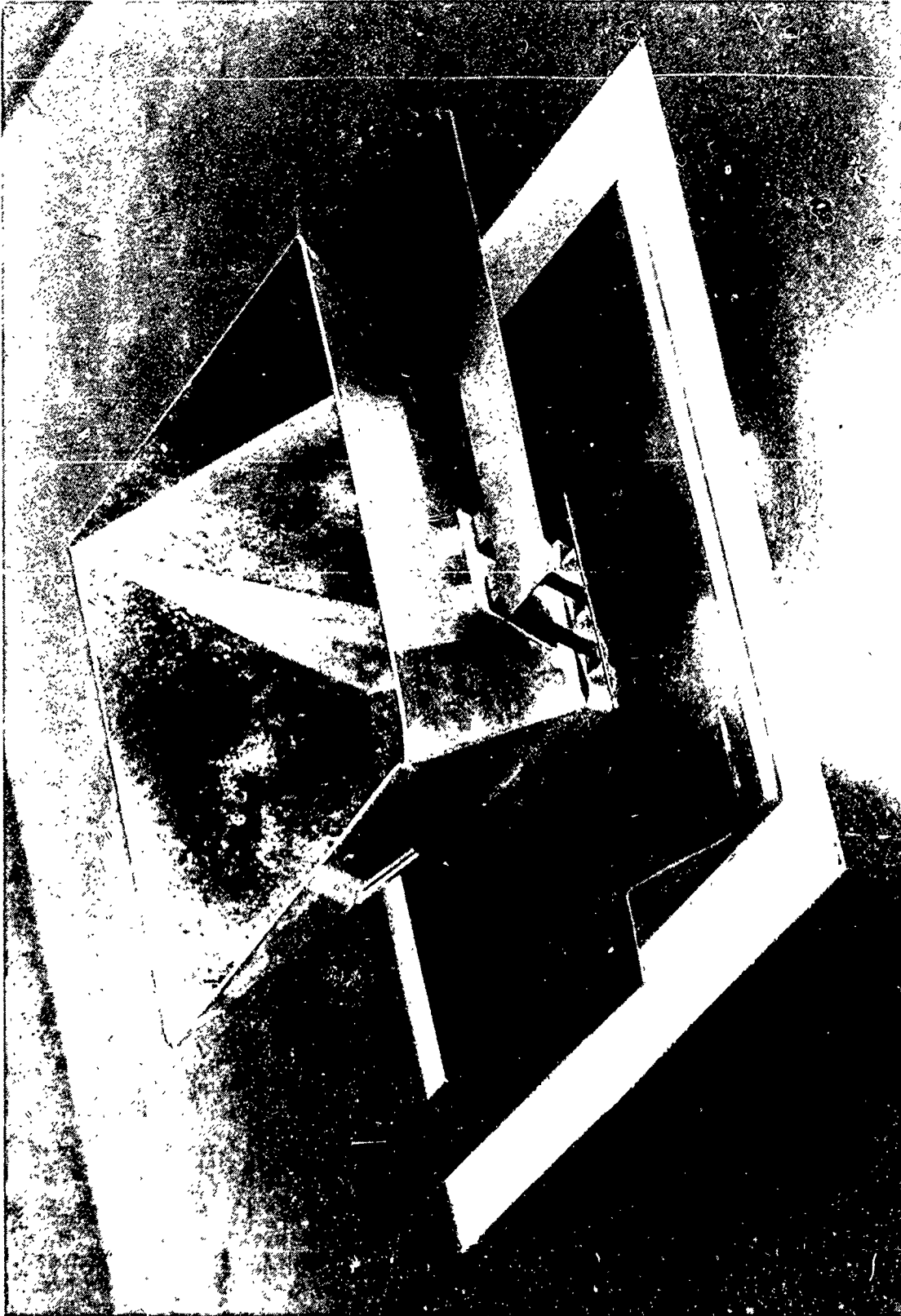
FIGURE 4. — Solar Concentrator Cell Assembly Bonded with Type II Adhesive Tape.

Photo Courtesy of Sandia National Laboratories.

Thermally Conductive
Silicone Rubber .008″-.015″

SMT Component

Circuit Board:
Polyimide/Kevlar

Aluminum
Heat Sink
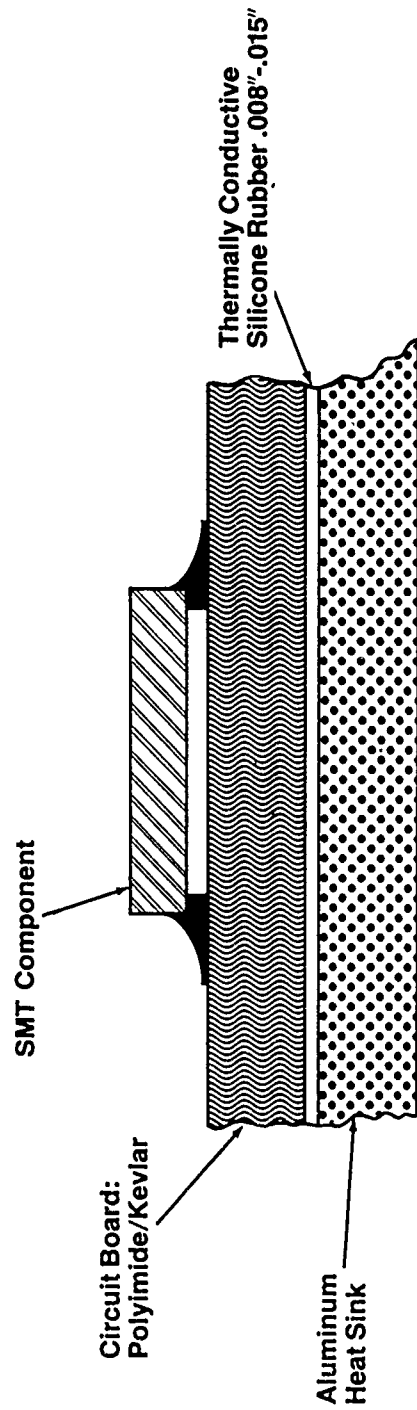
FIGURE 5. — SMT Board Bonded with Type III Thermally
Conductive Silicone Elastomer.

Leaded Component

Circuit Board FR4

Aluminum Heat Sink

Thermally Conductive
Silicone Rubber .030"-.060"
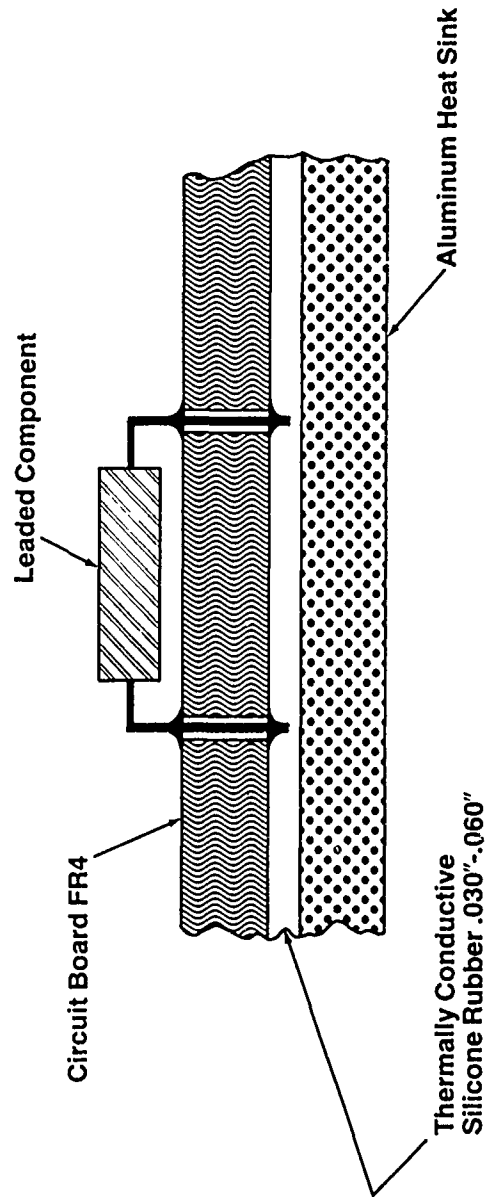
FIGURE 6. — Through Hole Board Bonded with Type III.
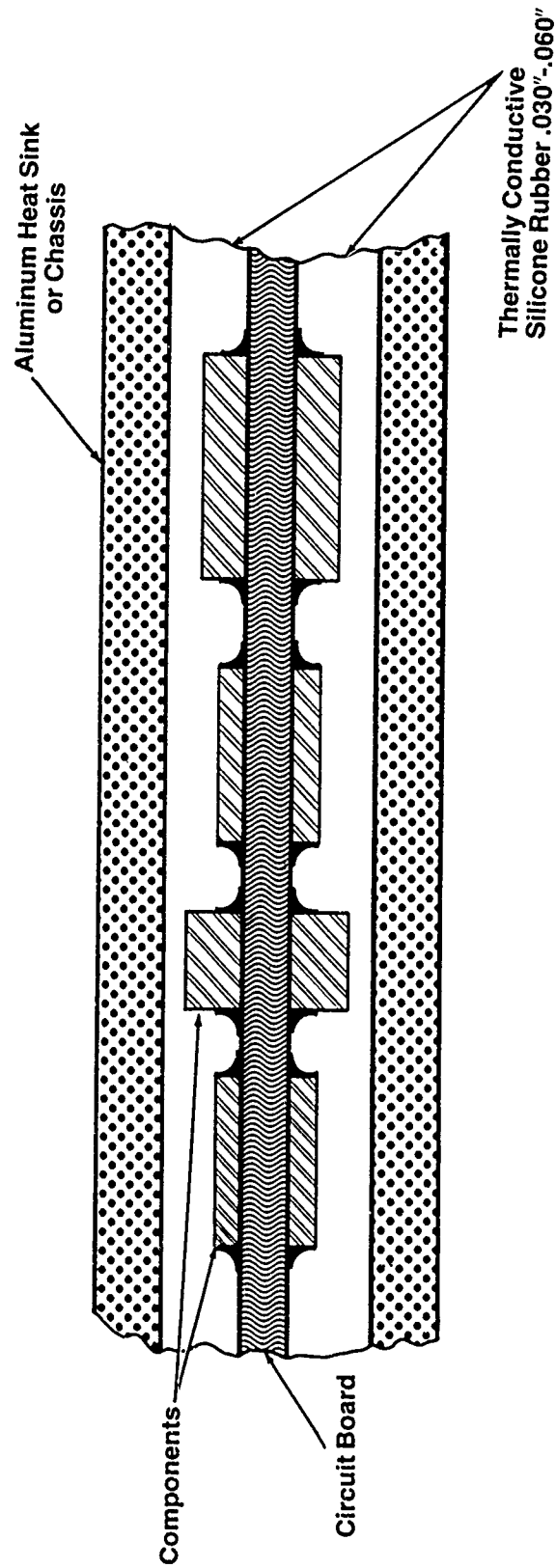
FIGURE 7. — Type III Used for Heat Sinking via Component Side.

ACKNOWLEGEMENTS

BIBLIOGRAPHY

Frauenglass, E, Moran, J., and Batson, R. "New Adhesives Speed Heat Removal", *CIRCUITS MANUFACTURING,* Feb. '84 pp. 91-96.

Dominic, C. "How to Select Adhesive Film for Heat Sink Attachment to PWBs", *ELECTRI-ONICS,* Mar. '87, pp. 48-49.

"Packaging and Assembly Materials Specification Guide", *ELECTRONIC MANUFACTURING,* Nov. '87, pp. 43-44.

Beavis, L.C., and Moss, M., "Thermally Conductive Silicone Based Materials for Attaching Concentrator Solar Cells to Heat Sinks", *AIChE Symposium - Heat Transfer,* Denver, CO, '85.

Buchbinder, M., "Choosing an Effective Adhesive", *CIRCUITS MANUFACTURING,* Apr. '87, pp. 28-34.

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THE NEED FOR CUSTOMIZED REPAIR

TECHNIQUES OF CONFORMALLY COATED

CIRCUIT BOARDS

By

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Abstract

This study deals with adapting various repair technologies to the
requirements of conformal coated printed circuit boards. Information
was gathered from both military and industry sources in an effort to
find best method examples, the culmination of which is reported in this
paper. Repairability of conformally coated printed circuit boards is a
prime concern of the electronics industry and is rapidly becoming a
technology in its own right.

h.... ··)8C addresses the different types of conformal coating

materials and the thicknesses required to conform with the parameters

that insure adequate and expected results from various conformal

coating types. These types of conformal coatings exhibit differing

characteristics and within these unique differences the electronics

industry finds the opportunity to select a conformal coating based upon

individual application needs. For example: high temperature

requirements point the user toward the silicones. Ease of removal to

the acrylics, structural strength to the epoxies and polyurethanes, and

least component stress to p-xylylene. The selection process for a

conformal coatings look at these factors and more, in an attempt to

optimize the final product in the areas of environmental isolation.

Various methods of removing conformal coating generally fall into four

methods: chemical, thermal, mechanical and gas plasma. This would

appear to be straight forward, yet the application of technology within

these processes or combination of processes is where the repair process

either finds success or failure.

The removal of conformal coatings by chemical means runs the course of

complexity from a chlorinated solvent to remove acrylics to the use of

Chloronaphthalene at 180°C to remove p-xylylene, and one can easily see

that the more resistive a conformal coating is to environmental hazards

the less receptive it will be to chemical removal. In the chemical

removal of the more tenacious conformal coatings the difficulty is due

to the lack of selectivity in the solvents. This simply means that the solvents are unable to tell the difference between conformal coatings and circuit board materials.

The removal of conformal coatings by the application of heat is most applicable to the families of epoxy, polyurethane, and p-xylylene. In these cases the material is either softened or degraded by the addition of heat. Difficulties encountered tend to come from again selectivity, but in this instance the selectivity comes from the area of degraded conformal coating between the destroyed material, degraded material and the material to be left intact. This degraded material is usually removed by mechanical means back to the pristene material in order to re-establish barrier integrity subsequent to the rework.

An additional difficulty in the removal of conformal coatings by thermal methods is the generation of smoke and toxic or noxious fumes. This requires that steps be established to stay within E.P.A. and O.S.H.A. guidelines.

Mechanical means find application in the conformal coatings which do not lend themselves to removal by the chemical or thermal methods. This implies that mechanical methods can be utilized effectively on all conformal coatings with the exception of acrylics which can be removed readily by a chlorinated solvent bath.

Mechanical methods, include many technologies including: ball mill, hand chisel, rubber impregnated with metal oxide, particle blasting, and water blasting. Each of these methods has distinct advantages and disadvantages and additionally tend to fit best with the particular conformal coating. The rotating ball mill readily removes hard, thick materials, but care must be taken to control the depth and direction, consequently the most often used method is to remove the majority of material with the ball mill and the remainder of the material with a chisel. The hand chisel is most often used with heat on the epoxies and polyurethanes or as a shovel on the silicones shearing and lifting out the material. The chisel also is used on the p-xylylenes with heat to scrape the material from the substrate.

The metal oxide impregnated rubber abrasive tool is used to clean the substrate of small amounts of conformal coating. It works quickly but can become clogged with waste residue so its use should be kept to removal of small amounts of material. It is important to maintain slow R.P.M. on the tool to minimize heat buildup at the contact point. The slow R.P.M. also minimizes static generation although the tool should be grounded at all times to minimize potential E.S.D. damage.

Particle blasting find application in removing all of the harder types of conformal coatings, but has the disadvantage in that it it's ability to remove material is non-selective and component and substrate damage

is possible making the operation operator dependent. The major

disadvantage is that particle-blast residue is left behind and imbedded

in the surrounding conformal coating. To entirely remove this material

is difficult at best and therefore, the process is not used to best

results for selective stripping.

Plasma removal applies primarily to p-xylylene conformal coatings

various gases and combinations of gases are used throughout the

industry and most businesses consider this information proprietary due

to the time involved to find a prescription to the problem. Plasma

etching is very effective but strip rates are the relationship between

the function of gas type, wattage, part temperature and chamber loading

density. This complexity of parameters offers the operator a great

deal of latitude within this process and consequently the efficiency

can be fine tuned. Plasma etching can be made highly selective by

masking, allowing only a portion of the p-xylylene to be exposed to the

plasma. The selectivity, however, is dependent upon the gas tight seal

of the masking and therefore, care must be exercised to maintain

precise edge control of the selective stripping.

A major concern in the repair of conformal coated circuit boards centers

about the positive identification of the coating. Hard polyurethanes may

resemble acrylics and soft urethanes resemble silicones. To the

unfamiliar eye p-xylylene coated circuit boards appear to have no

coating at all. Repair technicians may be faced with the repair of

many different types of conformal coatings, and the first step is
identification of the conformal coating.

The decision chart listed in Figure 1 illustrates identification of
conformal coating types through the use of six physical
characteristics. A more positive identification is available through
chemical means (Lieberman-Storch-Morawski and Sodium nitroprusside test
results), or by standard methods of impaired spectroscopy.

Circuit board types primarily affect the repair procedure in the area
of component removal and replacement. Through hole leaded component
board designs utilize solder processing on the side of the circuit
board opposite the component. Typically the solder is extracted from
the hole, freeing the lead prior to removing the component. In surface
mount designs however, the solder must be heated to liquid stage
simultaneously with the removal of the component. This difference in
design is most obvious but yet many times ignoring this obvious
information leads to foil delamination, heat damaged components. Other
complexities of the repair function are found within the components on
the board. Passive components typically offer little threat to the
repair technicians abilities unless they are confined in close
proximity with other components.

Active components however, take on more sophisticated geometrics and their removal and replacement increases proportionally with the number of solder connections. Additionally the increasing size of component usually is combined with decreasing space between components and repairability quickly approaches the improbable if not impossible.

Designing a Repair Process for Conformally Coated Circuit Boards.

The previous sections have been directed at generalities of coating materials and at exposing the uniqueness of one board design to another in an attempt to illustrate that the individuality of design also demands a uniqueness of repair method. The repair method although created to work in a single area may not be the only method found to be acceptable. How many acceptable methods exist is an unknown, but the key to understanding here is in the word acceptable. Our objective is to restore the circuit board to its original condition, complete with all expectations of functionality and reliability, any reduction in usable life is not alternative.

The design of the repair process must then look at not only circuit design, but also at the availability of equipment and processes. It makes little sense to design a repair process that is unattainable although this happens more often than expected. The removal will have one set of problems, the replacement another and the process equipment

must possess adequate capability to accomplish removal and replacement

with a high level of repeatability.

The first step in designing a repair technology is to first look at

repair of the board without any conformal coating. Many times the

design is only marginally repairable in terms of the design parameters.

For example the maximum storage temperatures of adjacent components

cannot be exceeded with the removal and replacement of a component.

When this parameter cannot be attained on an uncoated circuit board

every time, the possibility of an acceptable repair method for

conformally coated circuit boards being developed is very unlikely.

When repairability has been established on the design, then and only

then can the repair process be expanded to include removal and

replacement of the conformal coating.

To remove acrylic conformal coatings the best choice of repair method

is chlorinated or fluoroinated solvents. Acrylics are easily removed

and damage to the board and its components is for the most part

unlikely, although verification should be made before adapting this

method.

In the case of epoxies the use of a ball mill is a good choice for

removal of the majority of material followed by heat softening with

thermal parting tool and a hand chisel to remove the remaining

material. When densities increase the work may require magnification

and extreme dexterity. Burning epoxy is not an acceptable method due to its non-selective nature and the possibility of charring or delaminating the circuit board, therefore soldering irons should not be used to heat epoxy. An alternate method of heating may be accomplished with hot air jet although the amount of heat varies with working distance and air volume making this more sensitive to operator skill. Abrasion methods of rotating bristle brush also may work for the final clean-up of the affected area.

Polyurethanes are best removed by mechanical means in a similar manner to epoxies however, the thickness of the coating will influence the method of removal. A very thin material can be removed with an abrasive wheel followed by an abrading with a rotating bristle brush. The procedure for removing thicker materials is to use a ball mill to reduce the material thickness to the point where the thin materials techniques apply. Another method involves a commercially available bullet-shaped nylon tip on a high torque/low R.P.M. tool. By varying the speed between 1,000 - 3,000 R.P.M. sufficient heat from friction is developed which will soften the coating while still providing sufficient force factor via the high torque. The nylon tip is pressed against the coating. As the material softens, and the tip enters the mass of the coating a pushing force is applied laterally through the coating to move it aside. The material bunches up from the printed circuit board and is slowly removed.

Silicone and soft polyurethane conformal coatings are best removed by a

peeling method. A dull blade is used to slit the material and to peel

it off the printed circuit board assembly. Additionally the use of

certain cleaning solvents: Trichlorotrifluoroethane TF,

trichloroethane or naphtha can be used to swell the material to ease

the peeling process however the use of chlorinated cleaning solvents is

not recommended near electrolytic capacitors. The soak, swell and peel

method may have to be repeated in order to completely remove the

material.

P-xylylene is a horse of a different color in the conformal coating

industry. Because it is built up upon all surface areas of the circuit

board while under vacuum, this coating encapsulates all solder joints,

wires, and components on all sides. P-xylylene will even penetrate a

.001 in space so its covering of the board is not subject to shadowing

as are the other coatings which are either applied by spraying or

dipping. Additionally para-p-xylelene is applied in a much thinner

coating, from .0006 to .002 inches per mil I 46058C. To remove a

leaded component a parting line is cut around the solder joint and an

air vent is opened around the solder joint on the component side of the

plated through hole. The solder is now heated through the material and

extacted using a solder extraction tool. With the component leads free

of solder the component can be removed. Any p-xylelene remaining under

the component can be removed using a low R.P.M. - high torque motor tool and a rubber-oxide bullet shaped abrasive tip. Tool speed should be within the 100 - 500 R.P.M. range and the device should be grounded to eliminate E.S.D. generation. Surface mount components are removed similarly by scribing a parting line about the component and simultaneously melting the solder connections and lifting the component free of the board. A note of caution because the p-xylylene surrounds the entire solder filet the lifting force required to separate the multileaded component from the board is increased to where a device cannot be raised reliably with a suction cup lifting tool. Because of this a mechanical lifting method is recommended. The thin nature allows solder to be heated and melted through the p-xylelene allowing for a relatively easy repair since material does not need to be removed to access the component. Care must be taken to insure a clean parting line between material to be removed and material to be left in place and at the same time not damage the circuit board by the cutting action.

After the component has been replaced the repair process now takes on some concerns as new production in regard to recoating the circuit board. Conformal coating by its nature requires high levels of cleanliness for adhesion to the substrate. Furthermore, contamination residues trapped under conformal coatings can cause circuit shorting as

well as corrosion growth. P-xylelene because of its molecular vacuum deposition minimizes this problem. However, any lack of adhesion is more visibly apparent with p-xylylene because of its more flexible nature. The cleaning process in all cases must therefore carefully match the cleanliness of the original process. After the cleaning process sufficient drying procedures must be incorporated to avoid moisture intrapment. Moisture contained under the conformal coating can cause latent problems of bubbling and measling. The best drying methods incorporate both heat and vacuum and care must be taken to recoat quickly after the drying process.

In summation to design an effective repair process the process must be tailored not only to the type of conformal coating but additionally to the design of the board. Too many times' the topic of repair is avoided until the project is behind the eight-ball and the methodology of repair is left to the creativity and ability of the repair technician. With proper planning nearly all repair problems can be avoided and project success insured.

(1) Does board appear to be coated?

No (1a) → **(2)** Does board glow under ultraviolet light?

No (2a) → Board is uncoated

Yes (2) → Parylene

Yes (1b) → **(3)** Place one drop of acetone on coating. Allow to sit for one minute then rub spot with cotton tipped applicator

(4) Is the coating removed or dissolved?

No (4a) → **(5)** Run fingers across coating

Yes (4b) → Acrylic

(6) Note hardness, texture, and ease with which fingers slide across surface

Hard, smooth; fingernail slides easily — (6a) → **(9)** Apply one drop of acetic anhydride followed by one drop of concentrated sulfuric acid (Liebermann-Storch-Moravski Test). Note colors that develop over a five-minute period.

Soft, rubbery; fingernail will penetrate surface — (6b) → **(7)** Burn two small pieces of the coating

(8) Note flame color, smoke, and residue

Black smoke, yellow flame, dark sticky residue (8a) → Soft Urethane

Smokeless, white flame, white ash (8b) → Silicone

(10) Gently heat two pieces of the coating in a test tube until vapors begin to rise from the piece. Insert into the test tube a strip of filter paper which has been moistened with an aqueous morpholine/sodium nitroprusside solution. Note colors that develop within 15 seconds.

Confirmatory Test ←

(11) Compare results of the two tests with the tables of Lieberman-Storch-Moravski and morpholine/sodium nitroprusside test results.

→ **(12)** Standard methods of infrared spectroscopy should be used when available. Compare spectrum of unknown coating with standard spectra provided in the IR manual.

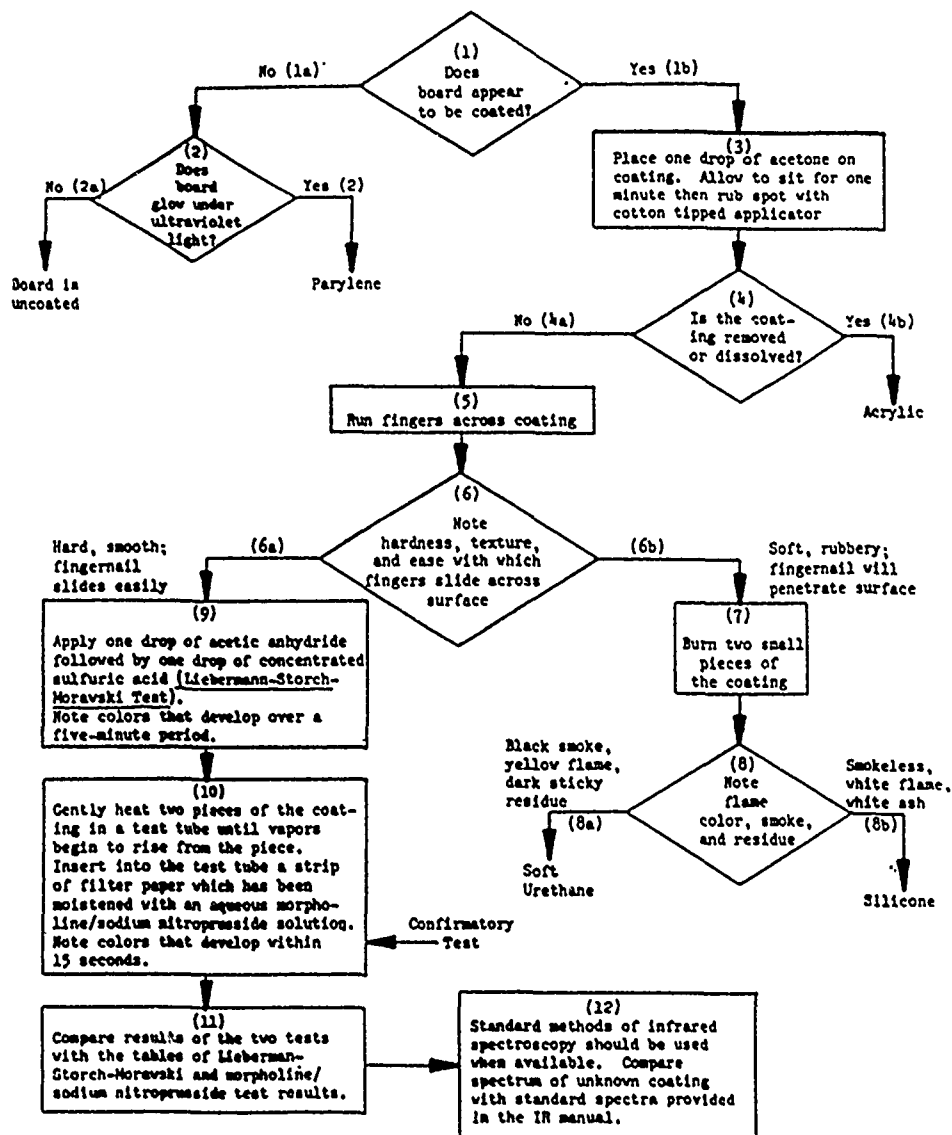Figure 1   Flow Diagram For
Identification of MIL-I-46058 Conformal Coatings
(Epoxy, Acrylic, Urethane, Silicone, Parylene)

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DoD/DLA/DESC HAZARDOUS MATERIALS MINIMIZATION (HAZMAT) PROGRAM

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INTRODUCTION

Environmental concerns are not new, but only in the past few years have they started to receive the attention they deserve. The Occupational Safety and Health Administration (OSHA) and the Environmental Protection Agency (EPA) have been leading the way by implementing ways of reducing hazardous wastes. For its part, the Department of Defense (DoD) is compelled to deal with critical Congressional inquires and adverse publicity associated with being branded as a large scale producer of hazardous wastes. In response to its many internal environmental problems, DoD is taking steps to minimize hazardous materials in every item or product that it manages or procures. Therefore, in conjunction with its subordinate commands, the Defense Logistics Agency (DLA) is developing an in-house Hazardous Materials Minimization (HAZMAT) Program. This program is charged with identifying and/or reducing hazardous materials in every DoD electrical or electronic item managed or procured. DESC's mission within DLA is to provide prompt, effective and reliable electronic spare parts support to our military services and federal civil agencies at the most reasonable cost to the public. The center also provides engineering support to the military services by standardizing electronic parts and encouraging their use in new designs. As part of the overall HAZMAT program, DESC is working to reduce hazardous materials in those items it manages for DoD. DESC's program is also aimed at developing product designs which promote the reduction of hazardous materials, eliminate their use, or allow for recycling. This mission pertains to the final product, the processes used during manufacturing and testing, and any by-products created by the manufacturing process. In order to get the job done, we are dedicated to the idea that hazardous materials can best be eliminated by reaching back into the manufacturing process to prevent its formation. We also believe that the interests of both the government and industry will be better served by a cooperative approach in the search for less hazardous alternatives. By sharing initiatives, knowledge, burdens and objectives, both government and industry can obtain the greatest benefits. This paper will discuss the DoD/DLA/DESC HAZMAT Program in detail.

THE DOD/DLA/DESC HAZMAT PROGRAM IS A RISK ASSESSMENT PROGRAM

Before the program is outlined, we must understand its framework. The Defense Department purchases large quantities of electrical and electronic items. At the same time, DoD recognizes its obligations to be fully responsive to the environmental concerns of Congress and the public. Other federal agencies, such as EPA and OSHA, have been working diligently to clean up the workplace and the environment. Virtually everyone has felt the effects either directly or indirectly of the costs of environmental protection and restoration. Therefore, DoD has decided to eliminate or minimize the risks of adverse environmental impact caused by military and commercial items procured by the government. This DoD program is not related to EPA or OSHA, but works within their guidelines. We will examine every material we use to see if it poses any type of hazard to individuals or the environments at any point in the life cycle, or in the life cycle of any of the processes or materials connected with the pre-manufacturing, manufacturing and assembly, testing, transportation, storage, and disposal steps. If we identify a potentially hazardous material used during processes, we shall look for suitable alternatives. We shall ask industry for its comments as well. Once industry has responded and we in DoD have come to a consensus, a final recommendation will be made. If DoD decides that it cannot justify the use of the hazardous material and suitable substitutes are available, the material will be eliminated from DoD electrical and electronic items. DESC is ready to make those changes to our standardization documents. When suitable alternative materials are not available, DoD will fund or initiate research directed toward identifying satisfactory alternatives. We feel that industry should also be involved in a similar program.

DoD/DLA/DESC HAZMAT PROGRAM

On February 6, 1987, Mr. Carl J. Schafer, Jr., former Deputy Assistant Secretary of Defense (Environment), created the Hazardous Waste Minimization Program to develop ways of dealing with all of the DoD hazardous waste sites within the United States, and prevent additional problems at DoD activities in the future. Mr. Schafer's directive was in response to the passing of several environmental laws which basically dictated that hazardous wastes must be "cleaned up." Hazardous wastes needed to be cleaned up for the following reasons:

a. Clean up reduces the risks to human health and environment and conserves needed resources.

b. DoD considers reduced cost and liability to be important practical reasons and compliance to be a legal requirement.

c. DoD's character as a governmental agency calls for a responsive attitude toward the environmental concerns of Congress and the public.

The DESC Hazardous Waste Minimization Program received its funding in April 1987 and was able to actually get underway in early July 1987. At that

time, a team with members from each impacted directorate within DESC was formed to begin the very difficult task of developing the program for electronic components managed by DoD. The team's task was to identify, reduce, design for recycle, or eliminate hazardous materials in every item that DESC manages or procures. From the outset of the program it was evident that in electronic components the ideal way o' eliminating waste was to keep it from being created. This meant that we would emphasize the removal of hazardous materials which were part of electrical or electronic items, or were used to produce or test those items. Since it is advantageous to have a program title which reflects the primary goal, DESC immediately changed the program name from Hazardous "Wastes" to the Hazardous "Materials" Minimization (HAZMAT) Program.

As the DESC HAZMAT Program grew, we saw the need to publicize what we were attempting to accomplish. Promotion campaigns were set up to brief vendors and manufacturers. At these briefings we let attendees know that while our program is not part of any OSHA or EPA requirement, it is compatible with the programs of both agencies. We emphasize risk assessment and up front minimization through source reduction rather than concentrating on clean up of wastes. This approach allows us to work more closely with industry in achieving our overall goals.

THE DESC FUNCTION AND ROLE

The DESC Engineering Standardization Directorate has reviewed over 8,000 standardization documents in order to identify the composition of the end items. We are examining these materials to determine which one, are more hazardous. Once we have completed the review of a item, should we find that it has a hazardous component for which a reasonable substitute is available, we will ask industry for its comments before we incorporate the substitute material into our standardization documents. We will then give industry the opportunity to comment upon the proposed substitution. If they agree, no additional justification is necessary, but if they disagree they must justify their position and/or provide us with another suitable substitute and justify their recommendation. We will allow everyone who is willing to work with us the opportunity to gain insight and potential profit from using less or non-hazardous materials in their products and processes. We are attempting to develop a cooperative atmosphere between DoD and industry in every area of our plan. We will attempt to ensure that all interested parties can benefit from the program. In addition to getting the very best HAZMAT substitutes available, those members of industry who take an interest in this program will be able to more easily assimilate the standardization document changes since they will have helped create them.

DESC's business practices are being examined to see if they can be optimized to meet the goal of minim. 'd use of hazardous materials. This means that in addition to the work the Engineering Directorate is doing, other areas of DESC are undergoing changes which will improve our ability to minimize hazardous materials. Our Technical Operations Directorate manages

the acquisition of nearly 1,000,000 commercial parts which are not covered by military specifications. Therefore, we are not certain of the materials or processes used to produce them. However, they still fall within our mission and ways must be found to minimize their contributions to environmental hazards. Our Technical Operations team members are responsible for monitoring every Material Safety Data Sheet (MSDS) and have established in-house procedures to handle this increased workload.

Taking into account the importance of having current MSDSs to assist in minimizing hazardous materials, we have come to the conclusion that all of these MSDSs need to be made into deliverable items in our contracts. We have taken steps to ensure that all data supplied by a manufacturer deemed to be propietary will not be released to anyone, even under the Freedom of Information Act (FOIA), because this information will fall under EXEMPTION 4 of the FOIA, 5 U.S.C. Section 552(b)(4) which exempts trade secrets or proprietary data. Other avenues are being explored which will allow suppliers who can prove that they are using less or non-hazardous materials in their manufacturing and testing processes to be rewarded with higher prices on their items without jeopardizing their chances for contract award.

We understand that these new concepts may cause concerns on the part of some suppliers. We have taken steps to ensure that this program is fair, and, since the environment is becoming an ever increasingly popular topic for discussion and clean up, we believe it will be difficult to justify the use of a hazardous material once it has been designated for removal. Nevertheless, our legal staff stands ready to assist in handling complaints, and DoD is prepared to respond whenever needed.

Our Supply Operations Directorate is developing procedures which will be used to review every item they manage in order to ensure that hazardous items are removed from our inventory as soon as less or non-hazardous ones are available. Cost and remaining supply of the hazardous items will be factored into the newly developed Supply Operations equation so that they know when to delete the hazardous item. Once eliminated from DESC's supply, the hazardous item will no longer be available for purchase within the government. We hope that this procedure will provide an incentive for suppliers to develop hazardous materials minimized items.

Our minimization or deletion of hazardous material will not result in a sacrifice of quality. Our Quality Directorate is prepared to ensure that quality is not impaired; they will work with the Defense Contract Administrative Service (DCAS) to have as much in-shop surveillance as required so that our performance and quality requirements are still being met even though the items are being produced with reduced hazardous materials.

INITIATIVES

1. We shall continue to promote our HAZMAT Program in such a manner that everyone working in the fields of manufacturing or selling electronics and electrical items will know that HAZMAT must be taken into account during every phase of product development or production.

2. Once a material or group of materials has been identified as hazardous and DoD has taken appropriate measures to restrict their use, we shall make appropriate changes to the standardization documents that DESC manages.

3. We shall emphasize that manufacturers should design their products to incorporate recycling of hazardous materials, wherever possible. Every effort will be made to make this a requirement for future purchases of electrical and electronics items within DoD, as well as to include it in all of its standardization documents.

4. For quite some time now, DESC has been concerned with the development of manufacturing and testing processes which minimize hazardous materials. Fortunately, we have now been able to gain the support of one of the nations most respected organizations to help bring these areas under our purview. The Electronics Manufacturing Productivity Facility (EMPF) is a detachment of the Navy and has become recognized as having an ability to work with industry and give assistance in implementing new electronic processes and testing techniques. The EMPF has joined our program as a full partner and team member; they will be working with us to evaluate the risks presented to DoD by potentially hazardous materials and will be testing potential substitutes. Additionally, they will be able to help industry use these new materials; plus they will be able to help design new items with a view toward recycling of hazardous materials. The EMPF has also agreed to help DESC work with various universities in increasing research aimed at eliminating or decreasing hazardous materials.

5. We have contacted some universities which have demonstrated an interest in HAZMAT. The response has been good, and it now appears that we will be able to incorporate our program into the curriculums of these institutions. Of special note is the fact that the University of California, Los Angeles (UCLA) has agreed to work with us to help further research related to our program. Their participation will complement the work of the EMPF; preliminary talks have been extremely promising. DESC will encourage the EMPF/UCLA interface because the results of their efforts will help create a better world for us all to live in. As other universities become more aware of our program, we plan to expand our requirements to allow them to work with us as well.

6. An up front HAZMAT review by the DESC HAZMAT Program Office (HPO) is now under consideration for all new materials proposed for incorporation into DoD electrical and electronics items; this review will minimize hazardous materials by not allowing it into DoD in the first place.

ACTIONS PENDING

POLYVINYL CHLORIDE (PVC)

Review has been completed. A recommendation has been made that PVC be eliminated from DoD electrical and electronics items.

BERYLLIUM OXIDE (BeO)

BeO is currently in the fact finding stage.

CLEANING SOLVENTS

Benchmark testing of cleaning solvents is underway for determining substitutes for Chlorofluorocarbons (CFC)s. CFCs need to be minimized per the Montreal Protocol. Several alternatives are under review with new water soluble cleaning techniques and biodegradable solvents as possibilities.

EPILOGUE

The DESC HAZMAT Program reflects a long term commitment by DoD and DLA to change the attitudes of personnel in government and industry in order to clean up the environment. Success will come from working together in a cooperative atmosphere to achieve a goal that we can all be proud of. There is an expression which we are confident nearly everyone has heard, "Pay me now - or pay me later." Well, maybe with the use of the DoD/DLA/DESC HAZMAT Program, if we pay now we won't have to pay anything later. We at DESC believe this is a goal worth striving for!!!

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RESOLVING SHORTCOMINGS IN THE AREAS OF ENVIRONMENTAL STRESS SCREENING, POWER SUPPLY RELIABILITY AND THE TEST, ANALYZE AND FIX PROCESS

by

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ABSTRACT

In the early 1970s, the Navy had serious concerns about the low operational readiness of its sophisticated weapon systems. The potential for high equipment failure rates during combat was an unacceptable prospect and the inability of maintenance to restore equipment to acceptable levels of reliability was well recognized. It was easy to identify the problems manifested by poor design, inadequate testing and a poor quality manufacturing process. It was much more difficult to develop and implement the technical disciplines required as corrective action. This paper discusses three specific areas of technical discipline [Environmental Stress Screening (ESS), Power Supply Reliability, and Test, Analyze and Fix (TAAF) Procedures] which have been used for over a decade with measurable success. However, the experience gained has uncovered some shortcomings and these also will be discussed along with actions being taken to improve these processes. Finally, the discussions which follow will also provide the publication status of two revised Navy P-Documents (Manufacturing Screening and Power Supply Reliability) and a joint Navy-Air Force Technical Brief on TAAF. These three guideline publications should prove extremely useful to anyone involved in the electronics manufacturing business.

ENVIRONMENTAL STRESS SCREENING (ESS)

BACKGROUND

The reliability of a well-designed product is usually degraded to some extent in manufacturing. To sustain the level of reliability inherent in the design, defects in both parts and workmanship must be discovered and corrected before the product leaves the factory. Otherwise, they will show up as product failures in service use with possibly serious military consequences and always with undesirable cost impact. Further, the discovery and correction of defects in the factory contributes significantly to the manufacturer's production costs ("hidden" factory), as do field returns for correction of defects under contract requirements and warranties. Both the Navy and its suppliers, therefore, have always had a vital interest in the most efficient and effective means for the earliest elimination of defects.

EMERGENCE OF ESS IN THE DECADE OF THE 70'S

Most Navy programs acquiring electronic devices and systems traditionally depended on the final acceptance test to catch manufacturing defects. Some contracts called out specific pre-acceptance tests (e.g., burn-in) for the primary or ancillary purpose of defect detection. For a variety of reasons, both technical and contractual, the vast majority of electronic devices and systems delivered to the Navy continued to contain manufacturing defects in parts and workmanship which could have and should have been discovered and eliminated in the factory. In addition, the factory process, and the acceptance tests which followed, continued to take longer to accomplish, consumed more dollars, and did not provide the reliability and quality desired. A better approach was needed and this led to the emergence of environmental stress screening as a viable alternative. As a result, Navy engineers, who had program approval authority, started to emphasize what continues to be the two most cost-effective manufacturing screens: temperature cycling and random vibration. Proven techniques for performing both types of screens were prepared by two space program contractors for inclusion in NAVMAT P-9492, "Navy Manufacturing Screening," a document published May 1979 and re-printed several times in response to popular demand. This P-Document served a definite purpose because it provided the first tangible guidance on stress screening.

Subsequent to publication of NAVMAT P-9492, the Institute of Environmental Sciences (IES) assumed a leadership role in promoting industry-wide acceptance of the concept of environmental stress screening. In fact, the IES formed an Environmental Stress Screening of Electronics Hardware (ESSEH) Technical Committee which is still active today.

SHORTCOMINGS IN ESS

As a result of the large amount of information and experience gained since 1979, the case for increasing ESS application grew stronger. However, several shortcomings were discovered which could be traced to certain misconceptions relative to screening theory and implementation. The shortcomings include, but are not limited to, the following areas:

- P-Document use as a contractual document versus a guideline document

- Most effective ESS types for flaw precipitation

- Application of ESS to development as well as production hardware

- Difference between ESS and acceptance testing

- Stress levels required and how to apply

- Baseline regimens for Thermal Cycling and Random Vibration

- Tailoring a screen

- Understanding thermal and vibration surveys

The IES/ESSEH Technical Committee, with support from the RM&QA Directorate in the Office of the Assistant Secretary of the Navy (Shipbuilding and Logistics), has initiated a revision to P-9492 to clarify existing misconceptions and to provide a body of knowledge which addresses the more prevalent shortcomings. Since publication of this revision is imminent, it seems appropriate to highlight some of the features of this updated P-Document which the reader should find interesting.

FEATURES OF THE NEW P-DOCUMENT

As with all P-Documents, this revision to P-9492 is not intended to be imposed as a contractual document. It is a guideline document which should be used in conjunction with the contractor's prior ESS experience, his facility capability, configuration of the hardware, etc., to satisfy the intent of any contractual requirements imposed. Similar to a handbook, it should serve as an aid in developing a viable ESS program. The guidance in this document focuses on assembly level stress screening. It makes the assumption that piece part quality levels meet requirements stipulated by the Navy. In this context the role of piece part quality is discussed. Also discussed is the effect of piece part quality on assembly yield with guidance on actions to be taken to ensure that piece part quality requirements are met.

Another feature of the revised P-9492 is the definition of environmental stress screening as follows:

Environmental Stress Screening (ESS) is a process which involves the application, to a product, of one or more specific types of environmental stress, either in combination or in sequence, on an accelerated basis, but within product ultimate design limits, in order to precipitate to hard failure, latent or incipient defects or flaws which, if left undetected, may cause unpredictable product failure in the Fleet environment, over the useful life of the product.

To understand clearly the concept of ESS and the contributions of this concept to the achievement of design reliability in production hardware, it was necessary to provide the above definition of ESS as a baseline. However, the emphasis on production hardware should not detract from the value of ESS during hardware design and development. For example, hardware used during OPEVAL/Navy Preliminary Evaluation (NPE) should be free of screenable flaws in order to permit an efficient evaluation and concentration on design and performance issues.

Further, it was necessary to describe in the revised P-Document the fact that ESS is not a test, in the sense of a qualification test, but a process for precipitating flaws in the factory which accomplishes two things. First, the flaws are corrected prior to delivery of hardware to the Fleet. Second, evaluation of the flaws and their cause factors leads to improvements in the design and manufacturing process, thereby reducing the "hidden" factory effect and its adverse impact on cost.

The subject of stress levels is a major difference between ESS and acceptance or qualification testing. It is important to choose the right specific environment and stress levels because, to be effective and timely, the stresses must be applied on an accelerated basis in an environment tailored to precipitate discrete types of latent defects while simultaneously guarding against hardware overstress. This involves a clear understanding of the characteristics of an effective stress screen as described in the revised P-Document.

BASELINE REGIMENS

Once the concept and definition of ESS are understood, it becomes necessary for a baseline regimen to be established and tailoring techniques to be understood so that screening can produce the desired results. Unlike qualification test environments designed to simulate fleet conditions and to produce failure-free operation, screening environments are designed to stimulate flaws to detectable failures and subsequent corrective action. Many small companies, because of their size and limited business volume, have not had the same opportunities to gain ESS experience as have large contractors. As a consequence, the following baseline regimens are considered to meet the minimum requirements for a Navy Environmental Stress Screening program:

- Temperature Cycling Stress Screening

- Random Vibration Stress Screening

Temperature Cycling Stress Screening

For Temperature Cycling Stress Screening, a baseline regimen is provided for three levels of assembly, i.e., PWBs/simple modules, units/complex modules, and systems. For each level of assembly, the following six characteristics are described in quantitative terms when appropriate (See Table 1):

- Temperature range of hardware

- Temperature rate of change of hardware

- Stabilization criterion

- Soak time at temperature extremes

- Number of cycles

- Equipment condition (power on/off)

The designer of the screening regimen can decide how severe or mild to make the baseline regimen within the recommended ranges and then control changes as necessary to accomplish the objective of precipitating latent flaws.

Random Vibration Stress Screening

For Random Vibration Stress Screening, the baseline regimen defines the characteristics of the excitation. It is generally agreed that an efficient screen will exhibit the following properties. First, the signal is broadband, i.e., a continuum of frequencies is present simultaneously all the time. Second, the frequency region over which it is important to achieve an appropriate spectrum level is from approximately 100 Hz to approximately 1000 Hz. Third, while continuous, the desired spectrum level need be only loosely defined and controlled providing a satisfactory overall level is achieved.

Next, the spectrum and overall level of the screen is defined. It is important to realize that it is the internal responses of the item which will precipitate the flaws even though it is the "input" which will be used to describe the screen and to control the vibration exciters. Thus, the measurement, in one form or another, of the internal response of the equipment is an important consideration.

For the LRU/LRM and SRU levels of assembly, the following five characteristics of a Random Vibration Baseline Regimen are shown, in quantitative terms in some cases, in Table 2:

- Power Spectral Density

- Axes Stimulated Serially or in Combination

- Duration of Vibration

- Power On/Equipment Operating

- Equipment Monitoring

TABLE 1. Baseline Regimen (Thermal Cycling)

CHARACTERISTIC	LEVEL OF ASSEMBLY		
	PWB*	UNIT**	SYSTEM***
Temperature range of hardware	-50°/+75°C to -65°/+100°C	-40°/+70° C to -55°/+85° C	-41°/+60°C to -55°/+70°C
Temperature rate of change of hardware	10°C/min to 20°C/min	5°C/min to 10°C/min	5°C/min to 10°C/min
Stabilization criterion	Stabilization has occurred when the temperature of the slowest-responding element in the hardware being screened is within 5°C of the specific temperature extreme.		
Soak time of hardware at temperature extremes - if unmonitored - if monitored	5 min Long enough to perform functional testing	5 min	5 min
Number of cycles	20 cycles to 40 cycles	12 cycles to 20 cycles	12 cycles to 20 cycles
Equipment condition	Unpowered	Powered, monitored	Powered, monitored

* PWB guidelines apply to individual PWBs and to modules, such as flow-through electronic modules, consisting of one or two PWBs bonded to a heat exchanger.

** Unit guidelines apply to electronic boxes and to complex modules consisting of more than one smaller electronic module.

*** It is up to the designer of the screening regimen to decide which elements (such as the parts, the solder joints, the PWBs, and the connectors) of the hardware must be subjected to the extreme temperatures in the thermal cycle. The temperature histories of the various elements in the hardware being screened are determined by means of a thermal survey.

TABLE 2. Baseline Regimen (Random Vibration)

Characteristics	Level of Assembly	
	LRU/LRM	SRU
Power Spectral Density (see Note 1 below)	6 GRMS (100 Hz to 1000 Hz)	
Axes Stimulated Serially or in Combination	3	2 (min) (see Note 2 below)
Duration of Vibration	10 min/axis	
Power On/Equipment Operating	See Note 3 below	No
Equipment Monitoring	See Note 4 below	No

Note 1: When quasi-random vibration is applied at the LRU/LRM level, random vibration is not required at the SRU level. However, subassemblies purchased as spares are required to undergo the same vibration required for the LRU/LRM level. An "LRU mock-up" or equivalent approach is acceptable. Vibration levels are the vibration levels that the unit being screened must experience. Vibration is usually measured by placing accelerometers on the unit(s) being screened.

Note 2: For an SRU, such as a printed circuit card, if only two axes are stimulated, one axis stimulated should be normal to the plane of the card, to assure that we are not just screening two basically symmetric axes and missing a critical orientation.

Note 3: Operation shall occur during the low to high temperature excursion of the chamber and during vibration. Equipment shall be operating at maximum power loading. Power will be OFF on the high to low temperature excursion until stabilized at the low temperature. Power will be turned ON and OFF a minimum of three times at temperature extremes on each cycle.

Note 4: Instantaneous go/no-go performance monitoring during the stress screen is essential to identify intermittent failures. If such monitoring cannot be performed for one level of assembly, ESS will be performed on the next higher level of assembly, but using ESS specifications of the lower assembly, if they are more severe and do not exceed the design limits of the next higher assembly.

TAILORING

For those who have the experience and expertise, and desire a more precise screening program, guidance on specific tailoring processes is discussed.

An integral part of any screening program is the "tailoring" process. Throughout this paper, we have discussed the importance of developing screens which stress the hardware to the level necessary to precipitate flaws but not to a level which will cause damage. Once a starting regimen is established, the iterative process of tailoring the screen continues as experience is gained and the screening process matures, whether it consists of thermal cycling, random vibration or a combination of both. Designing a screen is basically an empirical process — no cookbooks exist. In general, there is no such thing as a standard stress screen, although certain screens may be applicable to similar hardware configurations, especially at the PWB level of assembly. However, as a rule, an individual stress screen must be tailored to the hardware spectrum of interest.

SIMULTANEOUS SCREENING

Simultaneous random vibration and temperature stress screening is sometimes used but not essential. When temperature and vibration are applied separately, vibration should occur prior to the temperature cycle. For a chamber that has combined temperature and vibration capability, at least five thermal cycles should follow vibration. Required vibration levels are a response function and will be measured by accelerometers placed on the items being screened.

SURVEYS

Since surveys are an essential preliminary step in the development of tailored screening regimens, the remainder of this paper will discuss some basic considerations pertaining to Thermal Surveys and Vibration Surveys.

THERMAL SURVEY

A thermal survey is the measurement of the temperature histories of various elements in the hardware while undergoing thermal cycling screening. By evaluating the thermal response of the hardware to temperature changes in the heat transfer medium, the thermal survey helps determine the temperature history of the heat transfer medium required to produce the desired hardware thermal cycle. The survey is conducted as part of the development of the temperature cycling screening regimen. The purpose of the survey is to establish the following:

- Hardware temperature history in terms of temperature range and extremes, stabilization criterion, and soak time at extreme temperatures.

- Hardware elements to be subjected to the temperature history as a function of mass and thermal inertia.

- Method of heat transfer to the item being screened.

Experience with thermal cycling shows that flawed items fail in many fewer cycles than good items. Thus, a properly designed thermal screen will precipitate failures in flawed items while not consuming a significant portion of the useful life of good items.

Key Point

It appears, with the present state of knowledge, that thermal cycling acts differently on the different materials in an electronic assembly. Flaws in materials such as aluminum and copper are precipitated by rapid thermal cycling, whereas flaws in solder joints are precipitated by cycles with long dwells at high temperature. The designer of a thermal screen should keep this in mind and design the screen to precipitate the flaws expected in the specific hardware of interest.

VIBRATION SURVEY

A vibration survey is the measurement of vibration response characteristics at points of interest within an equipment when vibration excitation is applied to the equipment. Vibration surveys can be accomplished by using finite-element analysis or by placing accelerometers at points of interest. The basic purpose of a vibration survey is to measure internal response of the equipment to an arbitrary non-destructive input. Scaling is then used to calculate the screen input which will stimulate the desired response levels. Vibration surveys are particularly important to the establishment of single axis screens, two axes sequential screens, and simultaneous dual or triaxial screens, whereas three axes sequential screens are generally imposed without a vibration survey being performed since each axis theoretically will receive the same screen. Figure 1 depicts a flowchart showing the role of the vibration survey in the derivation of a vibration screen. More details on this flowchart as well as vibration survey guidelines are contained in the appendices of the revised P-Document.
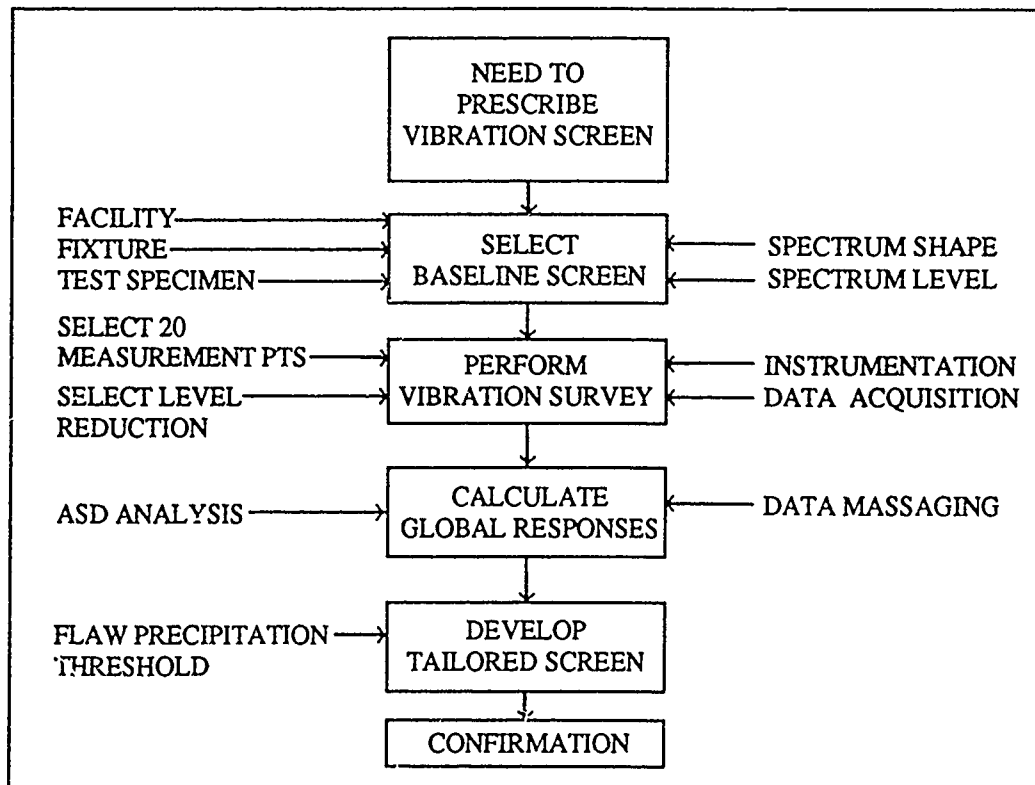

FIGURE 1. Flow chart of Vibration Screen Derivation

POWER SUPPLY RELIABILITY

BACKGROUND

Navy program reviews and fleet experience throughout the 1970s consistently revealed that the most serious and prevalent reliability problem with electronic systems was power supplies. In late 1979, the Deputy Chief of Naval Material for Reliability, Maintainability, and Quality Assurance requested that each Systems Command provide a list of power supply manufacturers from among its contractors and their suppliers. A subsequent letter sent to some 170 companies in 1980 highlighted the Navy's concern and sought assurance that adequate attention was being given to power supply reliability in accordance with the Navy's then-new reliability initiatives.

The industry replies to that letter pointed up four major problem areas: inadequate design analysis and derating; inadequate manufacturing screening; late design specification; and unqualified low bidders. The Navy responded by convening a Navy/Industry Power Supply Conference in Washington, D.C. on 2 April 1981 to discuss these problems and their potential solutions. The proceedings of this conference made it clear that the power supply problem was not a simple one and would require continuing effort to resolve.

Following the April 1981 conference, the Navy chartered a Navy/Industry Power Supply Ad Hoc Committee staffed by technical experts to identify the best design practices and manufacturing processes for overcoming the major shortcomings in low-voltage switching-mode power supplies. This committee met several times over the course of a year and provided the information which became the basis for NAVMAT P4855-1, Navy Power Supply Reliability, published in December 1982. In response to requests from industry and government, the Navy has distributed 18,000 copies of the original P-Document since its publication. As a result of the Navy's low-risk design and manufacturing guidelines and their implementation by industry, low-voltage switching-mode power supplies used in most military electronics are no longer high risk. Unlike conditions prior to the early 1980s, today's program and design reviews seldom highlight concerns relative to low-voltage switching-mode power supplies.

However, as the technology of both power supplies and electronics in general continued to advance, it became necessary to update the guidelines contained in the original publication to address improvements in low-voltage power supply technology as well as the shortcomings experienced with high-voltage switching-mode power supplies which are in the same high-risk state today as low-voltage power supplies were in the early 80s. The original Navy/Industry Power Supply Ad Hoc Committee was reconvened in 1986 and augmented by consultants in high-voltage power supply technology. The committee was charged with updating the original document and adding guidelines to overcome the major shortcomings in present day high-voltage switching-mode power supplies. The results of this effort were incorporated in the revised Navy Power Supply P-Document, NAVMAT P-4855-1A, dated January 1989 and they are summarized in this paper.

FURTHER ENHANCEMENTS TO LOW-VOLTAGE POWER SUPPLY GUIDELINES

The changes to the low-voltage sections of the P-Document are the result of improvements in design and component technologies over the last six years. The most significant changes to the guidelines are:

- Power density has been increased from 3 to 6 Watts per cubic inch.
- Power architecture of future 270 VDC power supplies is discussed
- Power density worksheet is provided to:
    - Determine the relative complexity of a low-voltage power supply package/design

Determine the volume required for the low-voltage power supply given the number of outputs and their characteristics as a function of the relative packaging density required by a system

The enhancements listed above will provide further guidance to a manufacturer when designing, manufacturing and testing low-voltage power supplies to maintain the high reliability power supply standards set in the original P-Document.

SHORTCOMINGS IN HIGH-VOLTAGE POWER SUPPLY DEVELOPMENT

Present day high-voltage power supplies are considered highly unreliable and are a major cause of system failure. Some of the more serious shortcomings include:

(1) High-voltage power supplies have well recognized, long-term degradation characteristics if corona and arc-suppression are not adequately addressed. Corona steadily degrades the primary insulation and field gradient design margin. The testing required to demonstrate the absence of these undesirable characteristics in a properly configured high-voltage power supply is both sophisticated and controversial.

(2) Contamination is probably the largest failure mechanism in high-voltage power supplies. Proper training of assembly personnel should be the first and foremost requirement. All assembly and test operations should be done in a controlled atmosphere wearing white (lint-free) gloves. The failure mechanisms of high-voltage power supplies are listed in Table 3.

(3) Components and assemblies are not being screened and burned-in at their operating voltages.

(4) High-voltage power supplies do not permit simple element replacement. Packaging constraints minimize the level of repairability within the power supply subassemblies. Manufacturing requirements force configuration control and repeatability of critical wire path routing. This greatly limits the ability of anyone not intimately familiar with a particular power supply from providing meaningful repair and replacement services.

Table 3. High-Voltage Power Supply Failure Mechanisms

DESIGN	MANUFACTURING
Geometry (Sharp Edge)	Contamination
Spacing	Component Failure
Corona	Multiple Dielectric (Various Materials)
Dielectric Breakdown	Voids (Potting Materials)
Dielectric Leaks	Component Handling (Cleanliness)
Compatibility of Materials	Encapsulant Curing Stresses

REDUCING THE RISK OF HIGH-VOLTAGE POWER SUPPLY I EVELOPMENT

In an effort to address these shortcomings, the Navy/Industry Ad Hoc Committee identified design and manufacturing fundamentals which should be considered in low risk development of reliable high-voltage power supplies. Designing and manufacturing high-voltage power supplies requires many additional disciplines beyond those required in low-voltage power supplies. The disciplines unique to high-voltage power supply development are:

- Corona Prevention
- High-Voltage Field Gradient Analysis
- Insulation Systems
- High-Voltage Field Testing
- High-Voltage Field Magnetics Design
- High-Voltage Field Manufacturing Disciplines

These disciplines must be practiced throughout the development of high-voltage power supplies. The revised Power Supply P-Document includes guidelines for applying these disciplines during the design and manufacture of reliable high-voltage power supplies. These guidelines are organized as follows:

(1) Design for reliability
(2) Design verification
(3) Manufacturing considerations
(4) Environmental Stress Screening

Design for Reliability

There are several key factors necessary for developing reliable high-voltage power supplies. Examples are highlighted in the following paragraphs, providing insight into potential problems and the techniques which are applied to high-voltage power supplies, i.e., those designs above 300 volts. Design and manufacturing techniques that apply to a reliable low-voltage power supply design also apply to high-voltage power supply designs.

Corona discharge is a predominant failure driver in high-voltage power supply equipment since it causes degradation of the insulation system. Corona reduction commences at the initial design phase and continues through manufacturing. A key element involves controlling the internal geometry to maintain an acceptable field strength throughout the assembly.

Degradation caused by corona can be reduced if materials are chosen carefully. A self-healing dielectric would be desirable but difficult to achieve. Oil systems are somewhat tolerant to arcs as the degradation products become dispersed. However, the degradation is still cumulative. Where the system dielectric is a gas or vacuum, arcs or corona can cause damage between interconnects and between components. Vacuum components such as traveling wave tubes, vacuum relays, vacuum capacitors, vacuum triodes and diodes can withstand a number of internal arcs without failure. Corona in solid dielectrics, which usually occurs at dielectric interfaces or voids, is cumulative and eventually results in destructive and catastrophic failure.

The ability of a system to tolerate an occasional arc is an essential part of a viable, high-voltage design. Circuit design and packaging techniques play a key role in the ability to tolerate an arc. Most designs limit current available to an arc through inductive di/dt or resistive limiting combined with current sensors and rapid turnoff.

Conservative design practice dictates that the output should be capable of surviving a shorted or open output, without degradation, for an indefinite time.

Design Verification

Development Testing. High-voltage power supply testing differs from that required of low-voltage power supplies during the development cycle. The selection of high-voltage insulation requires verification of design margins for both mechanical and electrical disciplines. Development testing of first-article units during the design phase is necessary to uncover inherent design and manufacturing defects before designs are committed to production. Standardized tests for high-voltage components, subassemblies and complete power supplies are rare. Lack of uniformity in specifying and screening high-voltage components has contributed to significant reliability problems in many programs.

Materials Testing. All insulating materials used in the fabrication of high-voltage power supplies should be subjected to inspection in accordance with the applicable material specifications. Table 4 summarizes those tests which should be performed as a part of the design verification testing for the selected insulating system.

Component Evaluation. The quality and reliability of high-voltage power supplies can only be as good as the components contained within. Therefore, components must be thoroughly evaluated to ensure that they meet required reliability levels and that all materials used in the fabrication of the devices are compatible with the overall system.

Power Supply Tests. The following design verification tests should be performed:

(1) Corona level

(2) Leakage current

(3) Assessment of design margins at worst-case operating conditions

(4) Temperature cycling/shock

(5) Arc tolerance

TABLE 4. Insulating Material Tests

TEST REQUIREMENT	INSULATION SYSTEM		
	SOLID	LIQUID	GAS
TENSILE STRENGTH	YES	NO	NO
HARDNESS	YES	NO	NO
COEFFICIENT OF EXPANSION	YES	YES	NO
THERMAL CONDUCTIVITY	YES	YES	YES
DIELECTRIC STRENGTH	YES	YES	YES
VOLUME RESISTIVITY	YES	YES	YES
DIELECTRIC CONSTANT	YES	YES	YES
DISSIPATION FACTOR	YES	YES	YES
ARC RESISTANCE	YES	YES	YES
GLASS TRANSITION TEMP	YES	NO	NO
ADHESION	YES	NO	NO
FLASH POINT	NO	YES	YES
VAPOR PRESSURE	NO	YES	NO
REVERSION RESISTANCE	YES	NO	NO
POUR POINT	NO	YES	NO
OTHER PROPERTIES (AS REQUIRED)	YES	YES	YES

If the high-voltage power supply is designed such that the electrical field stress exceeds the Corona Inception Voltage (CIV) of air, a temporary insulation, using either gas or a liquid, must be used when performing in-process tests. Materials that can be used for this type of test include sulfur hexaflouride gas or fluorocarbon liquids. Requirements for liquids or gases used during testing are:

(1) They do not contaminate surfaces or leave films.

(2) They are compatible with the materials used in the power supply.

(3) They do not produce ionic contamination under normally expected discharge levels.

(4) They have a high dielectric strength.

(5) They can be easily and completely removed after testing by heating or vacuum drying.

The most meaningful measure of insulation integrity is the AC voltage at which significant, sustained partial discharges (or corona) occur. This is called the Corona Onset Voltage (COV). In all cases, the COV shall be greater than the operating voltage. Repeatable, distinct corona activity can be seen in most insulating media at AC voltages considerably lower than in the DC case. Voids, fractures, separations, delaminations and other defects can be observed with AC testing which is not possible using any other method. Several manufacturers of partial discharge test equipment have been successful at detecting low-level corona (in the order of 0.1 to 1 picocoulomb (pC)) with practical, cost-effective equipment. The more successful high-voltage designers and manufacturers have used this equipment to:

(1) Understand basic corona phenomena.

(2) Compare different types of materials, components, subassemblies, processing, etc.

(3) Provide a consistent screening tool for research and development, production and "health" checks of finished components and equipment.

Environmental Testing. Environmental testing of high-voltage power supplies will generally follow the same guidelines as required for low-voltage power supplies. The additional tests required over and above those required for low-voltage power supplies are:

(1) Arc Testing - which may create localized high temperature and a possible fire danger.

(2) Pressure Vessel/Explosion Testing - mainly used when liquid or gas dielectrics are used, both of which require containers that may or may not be pressurized.

(3) Leak testing if pressurized.

The external connections to the high-voltage power supplies must be designed to withstand at least two times the rated output voltage for use in various test configurations such as:

(1) Vibration tables

(2) Temperature chambers

(3) Altitude chambers

(4) EMI test facilities

(5) Explosion chambers

The connections must be 100% tested prior to mating with the high-voltage power supplies and the test fixture should be designed to ensure operator safety at all times.

Manufacturing Considerations

Four necessary ingredients to achieve reliability in high-voltage power supplies are:

(1) Dedicated facilities

(2) Receiving inspection

(3) Detailed procedures

(4) Special personnel training

Dedicated Facilities. A typical facility for solid encapsulant fabrication and test is shown in Figure 2. The area should be a clean, controlled-access area. This will prevent unwarranted traffic through the area and prevent contamination by untrained personnel. Contamination can cause many failures in a high-voltage power supply even though the best materials and components are applied. The controlled area contains the following:

(1) Receiving inspection

(2) Storeroom

(3) Necessary workstations

(4) Inspection station

(5) Separate potting facilities for epoxy and silicones

(6) Test facilities

Receiving Inspection. The receiving inspection area should have access to equipment for 100% testing of all high-voltage components and be capable of performing burn-in tests. Each class of component should be tested as follows:

(1) Capacitors

    a. Corona

    b. Arc discharge current

    c. Parameters

(2) Resistors

    a. Stability at rated voltage

    b. High peak current if used for current limiting

    c. Parameters

    d. Corona

(3) Magnetic Components

    a. Corona

    b. Insulation

    c. Parameters

(4) Insulating materials as required per specification

(5) Other components and subassemblies as required per the imposed hardware specification

The purpose of the receiving inspection test is to ensure compliance with the specification of all components used in the assembly of high-voltage power supplies. The tests are planned to eliminate premature failure and thus reduce rework time required for the repair of failed units.
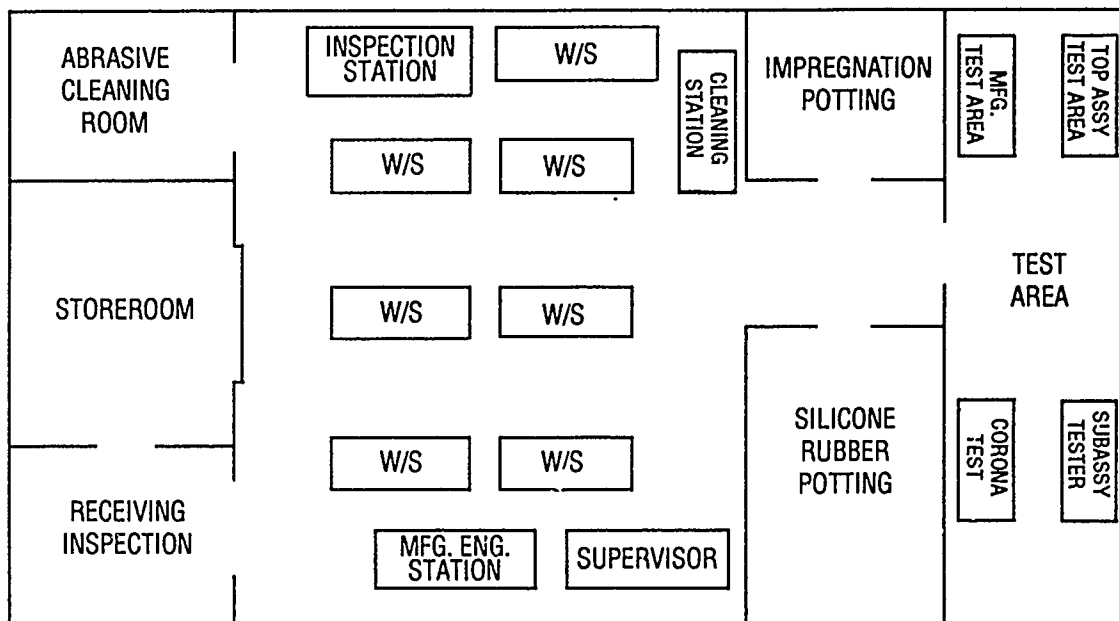
FIGURE 2. Typical Manufacturing Floor Plan

Environmental Stress Screening

Components. All components used in high-voltage power supplies should be screened to the requirements of this low-voltage power supply guidelines. Screening procedures for high-voltage components are the responsibility of the individual power supply manufacturer. The screening program must include, but not be limited to:

(1) Corona test

(2) Thermal cycling

(3) High-voltage burn-in

Subassemblies. All subassemblies shipped as spares must receive the same total ESS as those subassemblies procured as a part of a complete final assembly.

The final assembly of high-voltage power supplies should be subjected to ESS requirements specified for low-voltage power supplies, modified as follows:

(1) Following random vibration and 100% parametric test and prior to temperature cycling, an altitude test should be conducted, with continuous monitoring as follows:

a. 4 hours at altitude and minimum system operating temperature
b. 4 hours at altitude and maximum system operating temperature
c. 100% parametric testing per the customer's Acceptance Test Procedure

Design Review Checklists

Sample checklists are provided which should be used for high-voltage power supply design reviews.

TEST ANALYZE AND FIX (TAAF)

BACKGROUND

A recent study of development programs with reliability problems indicates a lack of understanding of the TAAF concept. Inconsistency impairs our efforts to use TAAF effectively today. It's an emotional issue. Some in the acquisition community remain unconvinced of the value of TAAF and violently oppose it. There is a lack of direction in applying it—little real technical guidance is available at the present time. Programs that do use TAAF are as likely as not to do it wrong, and this doesn't help sell it to the others. A lack of discipline has led to almost any test activity being called TAAF.

For example, Figure 3 illustrates how a current program used an approach to TAAF similar to that specified in MIL-STD-785B. This joint services program—some of the systems will be used on Navy platforms—is a classic case of doing everything wrong. The test articles were not the latest configuration and had not been screened for part and workmanship defects. The test was being conducted in four segments, with identified corrective actions incorporated in batches. Reliability verification tests (in effect, these were mini-REL DEMOs) were planned following the incorporation of each batch of changes, and a formal REL DEMO was planned at the conclusion. In between these batch changes and unnecessary REL DEMOs, no tracking of growth was attempted. Due to the abysmal failure of this TAAF effort, the government and the contractor are now scheduling a new TAAF program.

In contrast, Figure 4 shows the results of a TAAF program conducted on a torpedo sonar subsystem. The final in-water qualification test program was almost error-free and reliability is no longer a risk factor in this program. To perform this TAAF program, dedicated systems were fabricated for TAAF, and worst case environmental conditions and duty cycling were used. The TAAF growth plan used two alert lines drawn at a slope of 0.5 to mark thresholds for management attention. The actual test results were well above these lines, roughly at the same slope. Instantaneous MTBF values, based on the five most recent failures, were also plotted to aid in tracking reliability growth.

SHORTCOMINGS IN CONDUCTING TAAF

After reviewing a number of hardware acquisitions, it became apparent that the same problems were being repeated from one program to the next. The following is a list of many of these recurrent problems:

- It is essential that the program office have an understanding of the need and purpose of TAAF and provide strong support when necessary.

- To levy contractual MTBF requirements at certain points in TAAF testing is counterproductive since it will not encourage finding failures.

- A means of tracking contractor performance without providing a negative TAAF incentive must be used, such as defining an acceptable growth range for reporting purposes.

- Use of early hardware has drawbacks such as:

  - Hardware with tolerance or performance problems may be switched with TAAF hardware to allow performance tests to proceed.

  - Early hardware will contain early software; TAAF hardware may not be completely representative as software changes may be made which are not functionally compatible or easily installed in the older hardware.
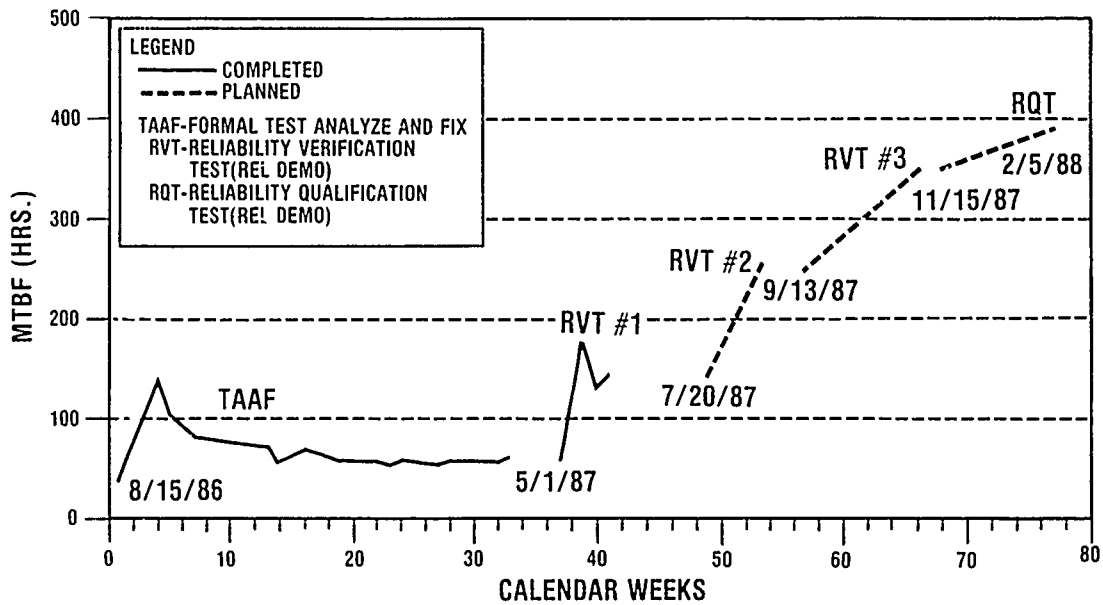
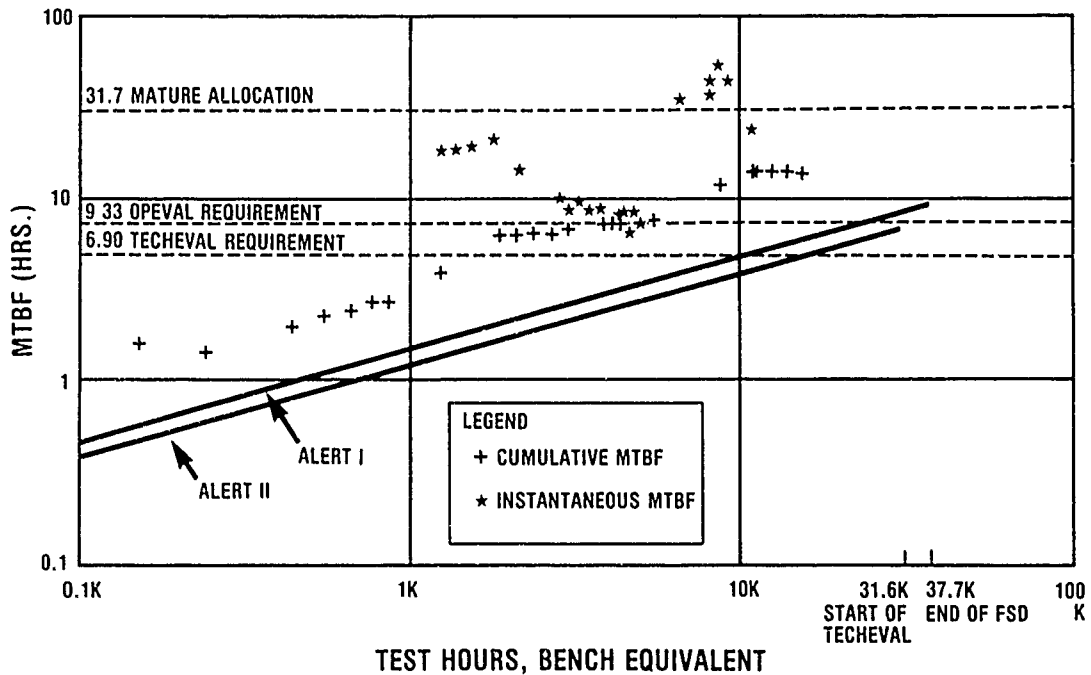**FIGURE 3. Unsuccessful Reliability Growth Program**

FIGURE 4. Successful Reliability Growth Program

- Test set and spare parts compatibility may also cause delays.

- If early hardware is used, plans should call for cycling in up-to-date hardware and the retirement of older hardware.

- Holding on to assets is difficult and should be a major consideration in planning any TAAF Program.

- Using a large number of test specimens to shorten TAAF test calendar-time duration might be counterproductive since time-dependent, environmental-stress-related equipment weaknesses would not appear.

- Accumulation of TAAF hours may prove more difficult than anticipated due to factors such as:

  - Repair turnaround times — A lack of availability of spare parts or failure analysis capabilities will greatly lengthen the repair cycle.

  - Test facility problems — if a new test facility will be used, chamber availability will probably be less than anticipated while bugs are being worked out.

- Spare parts and repair resources should be readily available to fix TAAF failures.

- Monthly planning meetings should be held to prepare for TAAF and to track hardware, software and test facility preparation.

- After the start of TAAF, monthly tracking meetings should be held to document test progress.

- TAAF progress should be briefed at weekly Program Manager's meetings.

WHAT IS TAAF?

The TAAF process is an iterative closed-loop reliability growth methodology which includes testing, analyzing test failures to determine cause of failure, redesigning to remove the cause, implementing the new design, and retesting to verify the failure cause has been removed.

The TAAF process is necessary because, even with the very best of modern engineering methods, initial designs for systems that are complex or involve new technology have reliability deficiencies that cannot be fully detected and eliminated through design analysis. The TAAF process surfaces these problems early and eliminates them before rate production.

The heart of the TAAF process is the identification of reliability weaknesses. The total TAAF process includes both formal and informal means for doing so. The formal aspect is called a Reliability Development Test (RDT) and involves dedicated long term exposure of system equipment to simulated mission profile environments. The informal aspect is the systematic identification of reliability problems found during other activities, such as component/subsystem development testing, systems integration tests, qualification testing, and flight testing. Both means are essential to the total TAAF process and are illustrated in Figure 5

DEFENSE SCIENCE BOARD RECOMMENDATIONS

The Defense Science Board Task Force on the Transition from Development to Production agreed in February 1983 that TAAF is a key requirement to achieving adequate system reliability. The Task Force
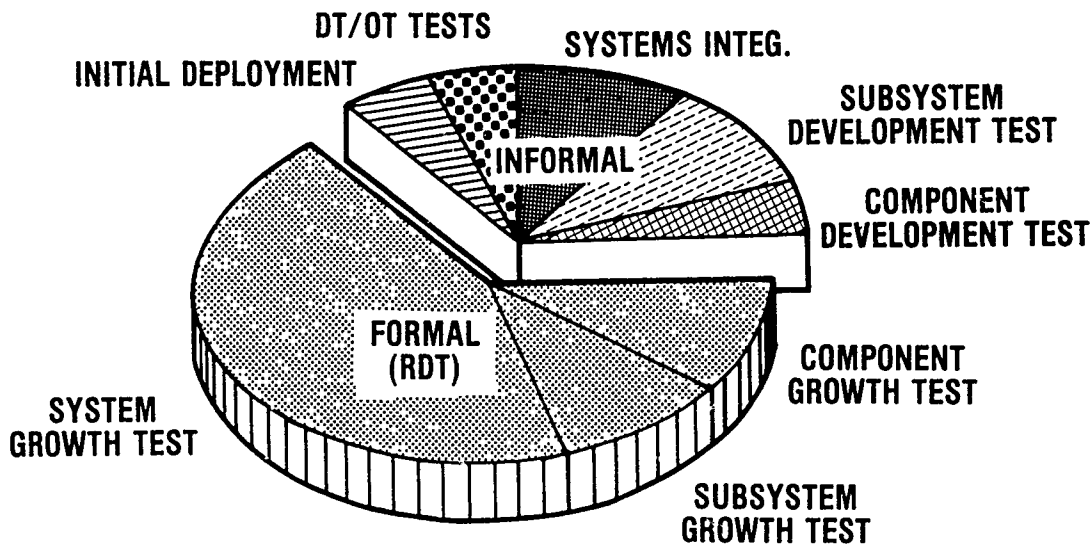
FIGURE 5. The Total TAAF Process

recommended tailoring to the needs of the specific program, flexibility to allow changes as the measured reliability data base grows, and integration with other development testing to maximize benefits at minimum cost. The Task Force recommended that selection of specific subsystems for TAAF be based on the subsystem's contribution to overall system unreliability, and that testing be terminated when the expected failure rate reduction from additional testing becomes small with respect to the system failure rate requirements.

These recommendations were among those incorporated in DoD Manual 4245.7-M which was published in 1985 period as a direct result of the Defense Science Board findings. The Navy's "Best Practices" Manual, NAVSO P-6071, was published in 1986 and elaborates further on the use and proper application of TAAF. More recently, we have seen the issuance of SECNAVINST 4490.2, which invokes Best Practices, including TAAF, in all Navy material acquisition programs. Currently the Navy is working with the Air Force on the development of a Technical Brief which will provide in a single, concise source document the methods most likely to result in a successful TAAF program.

CURRENT APPROACH TO TAAF

What are the elements recommended by the Navy for a successful TAAF program today? The following is a summary of our current approach.

First and foremost, a well-conducted TAAF program and sound environmental stress screening eliminate the need to run either reliability demonstration (REL DEMO) or Production Reliability Acceptance Tests (PRAT). Not only does this make more effective use of scarce test resources, but also if properly conducted, TAAF can provide a reasonable point estimate of achieved reliability.

TAAF is not a cure for marginally designed equipments. One cannot test-in reliability after having neglected classical design reliability disciplines, such as thermal analysis, failure modes and effects analysis, parts selection, stress derating, etc. TAAF is not a substitute for these disciplines but a necessary complement to a reliable design process.

Planning an appropriate duration for TAAF is perhaps the most controversial of its technical features. This is, of course, a major strength of the reliability growth model developed by J. T. Duane. A lot of actual test data has shown acceptable correlation to this model, and this is the primary reason we encourage its use. Nevertheless, indicated test time is so sensitive to selection of the slope and starting point that we recommend using all prior test data and analysis to establish these parameters. In the total absence of prior data, DoD 4245.7-M contains recommendations for default values. The problem is one of resource planning—early termination is always recommended when the requirement is met earlier than expected.

Three test articles seem to be typical of most TAAF programs, a compromise between cost, calendar test time, and the need for backups when a test article is down for analysis and repair or corrective action. The test articles should represent a mature design—no further engineering changes should be pending prior to conduct of TAAF. Failures due to bad parts and poor workmanship would add to cost and schedule while contributing nothing towards eliminating design shortfalls. Thus it is imperative that the test articles be constructed with fully screened parts, and that they be subjected to environmental stress screening prior to TAAF to find and eliminate workmanship defects.

The TAAF environment should simulate the mission profile as nearly as possible, including the full range and duration of environmental conditions. Each cycle of the TAAF environmental profile should follow the time phasing of the mission profile. Consolidating test time into fewer but longer times of separate environmental exposures could preclude discovery of failure modes triggered by a specific sequence in the mission profile.

I would say this about the failures that occur during TAAF: concentrate on eliminating the failure modes, not on counting the number of occurrences! Don't lose sight of the fact that the primary purpose of TAAF is to stimulate recurring failure modes for corrective action, not measure reliability.

FUTURE PLANS

So today we have this paradox in the Navy. We are aware of TAAF and its proven value, and we include it in our requirements, but we remain unable to take advantage of it in many of our programs. Some contractors know how to use TAAF effectively, and when we let them, we get good results. Other contractors are inexperienced with TAAF and we can offer little assistance at the present time. However, our long-range plans include formal training with emphasis on reliability growth and the development of a joint Navy/Air Force Technical Brief on TAAF. Training will get underway in 1989, and will be structured around the critical path templates outlined in DoD Manual 4245.7-M and NAVSO P-6071. In-depth treatment of each discipline will include the level of detail necessary to bring consistency into the Navy's use of reliability growth testing. The completion of the Technical Brief is expected by early 1989.

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PUBLIC LAND: RESOURCE FEATURES AND RECREATIONAL USE OPPORTUNITIES IN THE RIDGECREST AREA

by

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ABSTRACT

Public land in the vicinity of Ridgecrest, California covers extensive areas. Managed by the U.S. Bureau of Land Management and other agencies, this land provides opportunities for outdoor recreation, sightseeing, and backcountry exploration. Landscape diversity creates a tremendous range of natural resources which exist along with many historic cultural features. By following safety precautions, visitors can experience and enjoy a wide variety of recreational activities in scenic desert areas highlighted by many unique resource features.

RIDGECREST AREA PUBLIC LANDS

The U.S. Bureau of Land Management (BLM) is a federal agency within the U.S. Department of the Interior. The BLM is a multiple-use land management agency with responsibility for overseeing 272 million surface acres of public land - about one-eighth of the Nation. Most of this BLM administered land is concentrated in the western United States where large tracts occur primarily in desert areas and in Alaska.

The history of BLM managed lands is an interesting and complicated story related to numerous Congressional Acts, Executive Orders, and the changing views, needs, and activities of our citizens. Originally established by Congress in 1812 as the General Land Office, the agency was merged with the Grazing Service in 1946 and renamed the BLM. In 1976, Congress enacted the Federal Land Policy and Management Act which gave BLM a coherent legislative mandate as a multiple-use land management agency. Multiple-use means that BLM is responsible for sustaining renewable resources, allowing proper use of nonrenewable resources, and providing for the public use and protection of all public land values. This is frequently a controversial task

in the California desert where there are many diverse uses
and numerous resource values needing protection.

The 25 million acres of land comprising the California
Desert were designated by Congress in 1976 as the California
Desert Conservation Area in recognition of its historical,
scenic, archaeological, environmental, biological, cultural,
scientific, educational, recreational, and economic
resources that are uniquely located adjacent to an area of
large population (Reference 1). Approximately one-half of
the area - 12.1 million acres - is public land managed by
BLM under the guidelines of BLM's California Desert Plan
(Reference 2). This public land is under the jurisdiction
of BLM's California Desert District Office in Riverside,
California. Two and one-half million acres in the northern
portion of this area is administered locally by BLM's
Ridgecrest Resource Area Office - one of five resource area
offices of the California Desert District.

The Ridgecrest Resource Area's 2.5 million acres of public
land generally lie between the Sierra-Nevada mountains on
the west, the Nevada state line and Death Valley National
Monument boundaries on the east, the White Mountains to the
north, and concentrated private land tracts starting about
60 miles to the south of Ridgecrest. Major categories of
management work include recreation, livestock grazing,
wildlife, lands, wind energy, geothermal, wilderness, wild
horses and burros, cultural, minerals, fire suppression,
visitor information, and ranger patrol operations.

This area lies within the Mojave desert and mostly within
the distinctive Basin and Range geologic province with
alternating uplifted ranges and down thrust valleys along
parallel faultline systems. Contained here are a diversity
of landscape features and ecosystems which occur in playas,
salt flats, alluvial fans, riparian zones, rugged canyons,
and mountains exceeding 11,000 feet in elevation. This
portion of the Basin and Range geologic province is notable
for some of the greatest relief in North America, along with
extensive rock records accounting for most geologic time
periods going back for over two billion years of the earth's
history. Indicative of the diverse and sensitive resource
values found throughout this area, 20 Areas of Critical
Environmental Concern have been designated by BLM for more
intensive study and protection.

Adjacent to some of the BLM public lands in this area are
public lands managed by other agencies. To the east is

Death Valley National Monument, a large Basin and Range complex managed by the U.S. National Park Service. To the west and north are the Sequoia and Inyo National Forests where generally higher elevation and forested lands are managed under multiple-use policies of the Department of Agriculture. About 40 miles to the southwest of Ridgecrest is Red Rock Canyon State Park. It is a 7,000-acre area of scenic volcanic and sedimentary rock formations with extensive exposures created by the incising of an intermittent desert stream downcutting through the rock as it was uplifted along a faultline.

RECREATIONAL OPPORTUNITIES

Recreational use, exploring, and sightseeing by casual infrequent visitors and by repeat "desert lovers" is a major value of the Ridgecrest area public lands. Due to terrain diversity, tremendous ranges of surface relief, a rich mixture of geologic events, and a record of human occupancy for over 10,000 years, this area has much to offer both to the casual and experienced desert visitor. The following are some of the public land resource activities, resource features, and points of interest available for public enjoyment in the Ridgecrest area.

Backcountry Travel. Vehicle access is necessary to most activities and there are many miles of primitive, non-maintained vehicular routes which lead into backcountry areas. Some public lands are closed to all vehicle use for the protection of resource values, but most existing routes are available for public use. There are innumerable existing routes for conventional vehicles, four-wheel drives, motorcycles, all-terrain vehicles, and dune buggy use.

While most of the local and dune systems are closed to vehicle use to protect unique dune system ecosystems, the Olancha sand dunes, about 60 miles north of Ridgecrest, are open to vehicle riding. There are four sand dune areas locally which are closed to vehicles but open for hiking and scenic viewing. The Eureka Dunes, Stove Pipe Wells Dunes, Saline Valley Dunes, and Panamint Dunes are all distinctive with their own unique views. A "recent" geologic feature, these dunes formed after the last Ice Age ended 10,000 years ago and prevailing winds collected sand from the now dry lake beds of lakes which occurred in many area basins. Hiking and horseback riding are also popular activities

throughout the area   While developed trails are limited,
there are unlimited numbers of routes available, including
over 60-area peaks which are climbed regularly by desert
mountaineers.

Camping.   Primitive camping and overnight use of
recreational vehicles is allowed throughout the public
lands. Such camping provides opportunities for visitors to
enjoy the area's desert solitude and scenery. There are no
BLM developed campgrounds here but vehicle camping is
generally allowed along all existing routes. Camping is
not allowed closer than 600 feet to wildlife watering
sources so that wildlife can water when needed. Shooting
and hunting is allowed as permitted by State and local laws.

Mining. Many small and large, abandoned and current mining
areas exist here. The Rand Mining District, about 30 miles
south of Ridgecrest, consists of four desert communities
which display many mining artifacts alongside modern day
heap-leaching gold mining operations. Another large mining
operation exists at Trona. Here, salines deposited by the
Owens River during the Ice Age have been mined since the
1900s.

Fossil Falls.   A relic waterfall in lava exists about
30 miles north of Ridgecrest.   The now dry channel and
waterfall of Fossil Falls formed during the Ice Age when the
Owens River was flowing year round. Flowing from Mono Basin
and probably connecting periodically with the Colorado
River, the Owens River cut two 40-foot high waterfalls into
a basaltic lava flow. Today the incised channels and water
sculptured rock remains.

Desert Tortoise Natural Area.   A 24,000-acre nature
preserve, about 60 miles south of Ridgecrest, is managed
to protect desert tortoises and a concentration of other
plants and animals. The concentration of species probably
occurs because of a higher incidence of summer rainfall.
The preserve contains the highest known density desert
tortoise population which exceeds 200 per square mile in
some parts of the preserve. Studies are showing that their
numbers are declining because of a variety of impacts,
including illegal collection, predation, vandalism,
introduction of disease through the release of captive
tortoises, grazing, and being hit by vehicles. There is an
information kiosk with interpretive panels and trails on the
southeast side of the preserve along the Mojave-Randsburg
Road.

Trona Pinnacles. An outstanding example of tufa (calcium carbonate) deposits consisting of over 500 spires up to 140 feet in height are located about nine miles south of Trona. The pinnacles were formed underwater when springs flowed into a deep lake that existed in the basin during the last Ice Age. The process of deposition was slow and required thousands of years to accumulate and then become exposed after the lake dried up.

Pacific Crest Trail. This National Scenic Trail extends for 2,600 miles from Canada to Mexico and is available for hiking and horseback riding. Generally following the Sierra-Nevada crest west of Ridgecrest, numerous segments are accessible for short- and long-duration trips.

Darwin Falls. Although predominately very arid, the local desert has many riparian zones associated with short streams and springs. At Darwin Falls, about 70 miles north of Ridgecrest, there is a year-round, two-mile stream that produces a 30-foot high waterfall and important wildlife watering area. A short one-half mile hike up the canyon reaches to the falls.

Wilderness Study Areas. The BLM public land in the local area has been inventoried for potential wilderness areas. The inventory identified 12 areas totalling 861,000 acres of scenic, pristine public land which are being recommended to Congress as worthy of wilderness designation. These areas contain rugged and isolated tracts of pristine desert public land that as wilderness would be closed to vehicles and managed by BLM to preserve their natural qualities.

Alabama Hills. Located near Lone Pine about 90 miles north of Ridgecrest, this hilly area of granite boulders is the gateway to Mt. Whitney - at 14,495 feet the highest mountain in the Continental United States. A well developed trail starts at the Whitney Portal and winds its way for 11 miles to the summit. The Alabama Hills with the dramatic High Sierra backdrop have been used for the filming of many movies and television series.

VISITOR SAFETY

Visiting the public lands around Ridgecrest requires special attention to safety concerns. Much of the area is isolated, with a harsh environment, unmaintained roads, and often no

other people nearby for assistance. Different desert areas and different types of activities necessitate varying safety precautions. Be sure you are fully prepared for all possible travel emergencies if you leave frequently travelled roads. More detailed information regarding BLM administered public lands and safety precautions is available at the BLM Ridgecrest Area Office.

BIBLIOGRAPHY

1. Public Law 94-579. Federal Land Policy and Management Act of 1976, Section 601, 94th Congress, enacted October 21, 1976.

2. Bureau of Land Management. The California Desert Conservation Area Plan, 1980.

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